

Features

- Xilinx® Kintex® UltraScale™ FPGA
- Four 1.25 GHz 16-bit D/As
- Four DUCs (digital upconverters)
- Extended interpolation range from 2x to 1,048,576x
- 5 GB of 2400 MHz DDR4 SDRAM
- Programmable frequency synthesized sample clock generator
- Sample clock synchronization to an external reference
- Powerful DMA controllers for moving data
- PCI Express interface (Gen. 1, 2 & 3) up to x8
- Multi-channel synchronization with clock/sync bus
- Optional clock/sync generator for multi-board systems
- Optional LVDS port and gigabit serial connections for custom FPGA I/O
- Ruggedized and conduction-cooled versions
- Navigator® BSP for software development
- Navigator® FDK for custom IP development
- SPARK® fully-integrated development system
- Free lifetime applications support



Applications

- Complete radar and software radio interface solution
- Communication transmitter
- Radar transmitter
- Signal Jamming
- Waveform signal generator
- Analog I/O for digital playback



The Jade Architecture

Evolved from the proven designs of Pentek's Cobalt® and Onyx® families, Jade® raises the processing performance while lowering the overall power requirements by building on the Xilinx family of Kintex UltraScale FPGAs. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions as well as providing an ideal platform for user-created intellectual property (IP).

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 71871 factory-installed functions include four D/A waveform generator IP module for simplifying data playback, and data transfer between the board and a host computer.

Additional IP includes: a programmable interpolation IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory installed functions and enable the 71871 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.



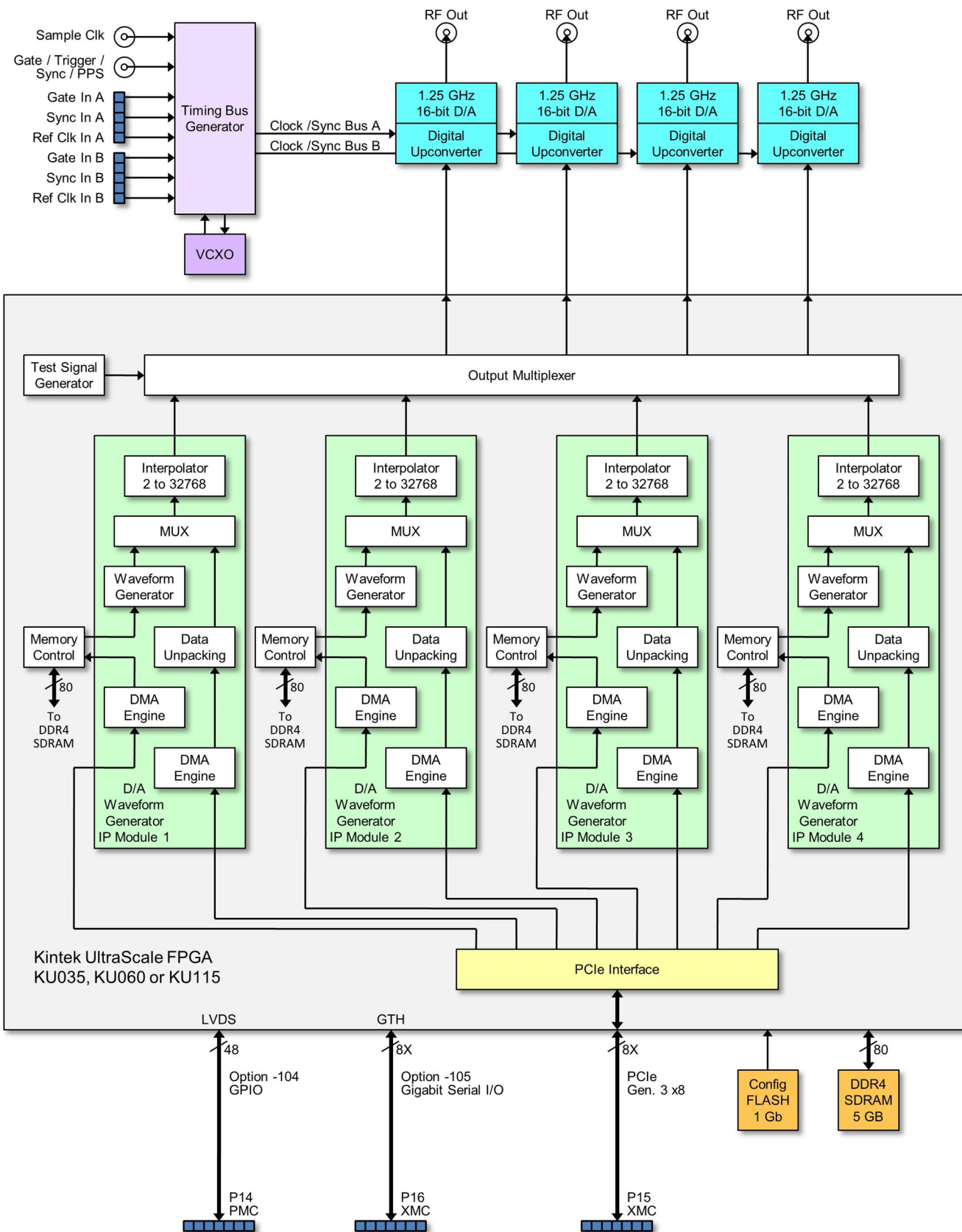
Xilinx Kintex UltraScale FPGAs

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs: KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.



71871 Block Diagram

Click on a block for more information.



D/A Waveform Generation IP Module

The 71871 factory-installed functions include a sophisticated D/A Waveform Generation IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71871 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel μ Sync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Models 7192 or 9192 Synchronizers can drive multiple 71871 μ Sync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The 71871 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

XMC Interface

The Model 71871 complies with the VITA 42.0 XMC specification. Each of the two XMC connectors provides an 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71871 supports x8 PCIe on the first XMC connector (P15), leaving the optional second connector (P16) free to support user-installed transfer protocols specific to the target application.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs P16 providing one 8X gigabit link between the FPGA and the P16 XMC connector to support serial protocols.

PCI Express Interface

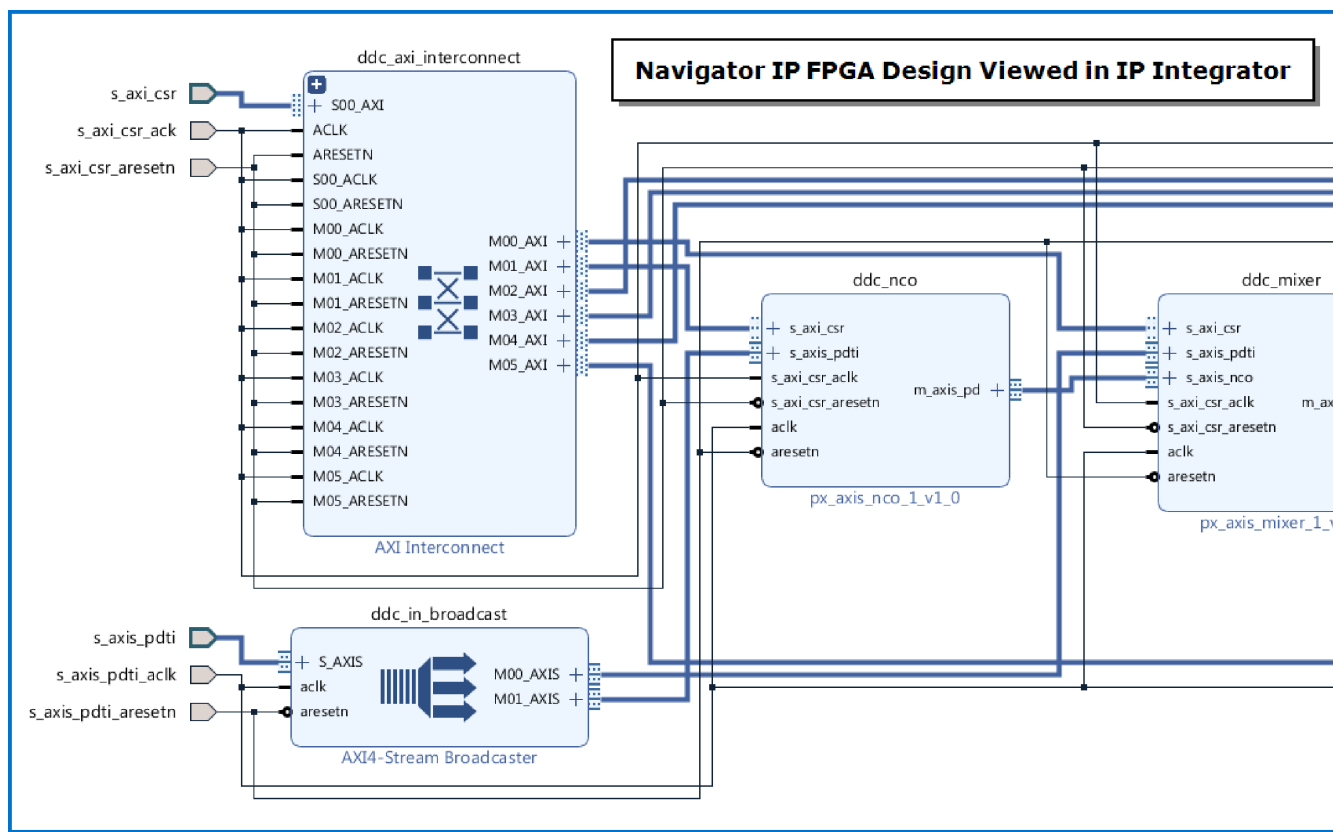
The 71871 includes an industry standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Navigator Design Suite

For applications that require specialized functions, the Navigator Design Suite allows customers to fully utilize the processing power of the FPGA. It includes an FPGA design kit for integrating custom IP into Pentek's factory-shipped design, and a board support package for creating host applications for control of all hardware and FPGA IP-based functions.

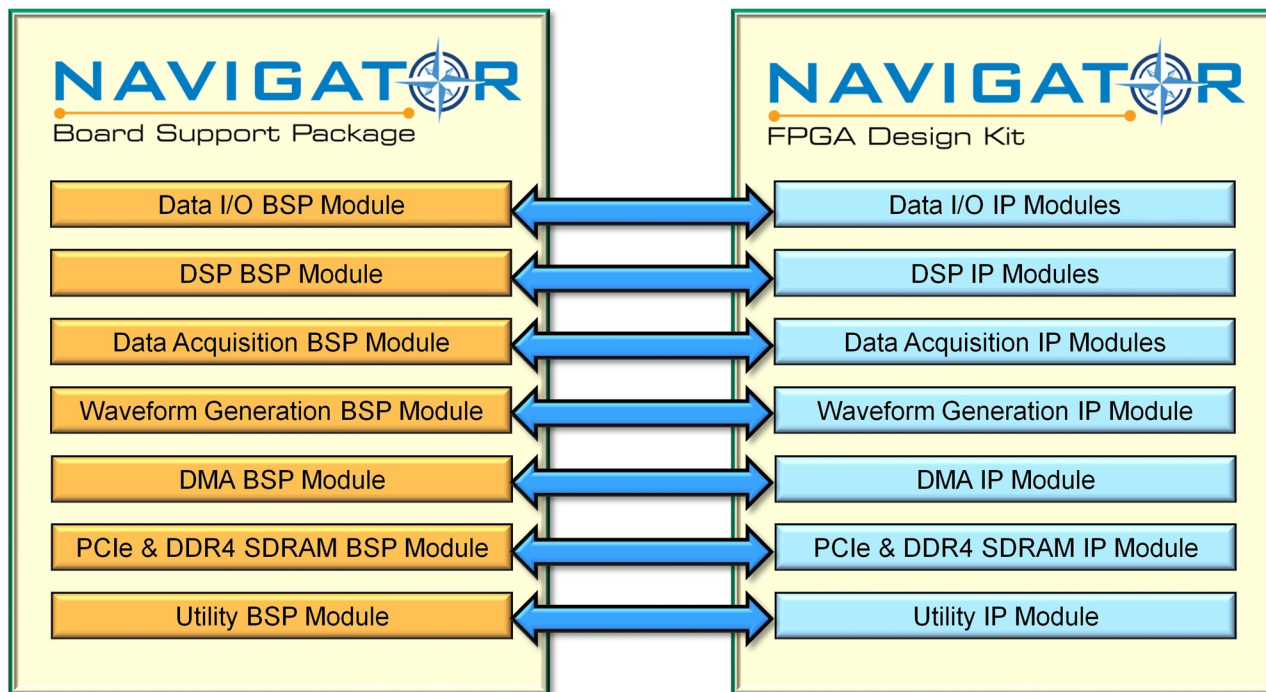


The **Navigator FPGA Design Kit (FDK)** for the Xilinx® Vivado® Design Suite includes the complete Vivado project folder for each Pentek product with all design files for the factory-installed FPGA IP. Vivado's IP Integrator is a graphical design entry tool that visually presents the complete block diagram of all IP blocks so the developer can access every component of the Pentek design. Developers can quickly import, delete, and modify IP blocks and change interconnection paths using simple mouse operations. Navigator FDK includes Pentek's IP core library of more than 100 functions representing a wealth of resources for DSP, data formatting, timing, and streaming operations, all based on the powerful AXI4 standard. Multi-level documentation for each IP core is a mouse click away, and fully consistent with Xilinx IP cores.



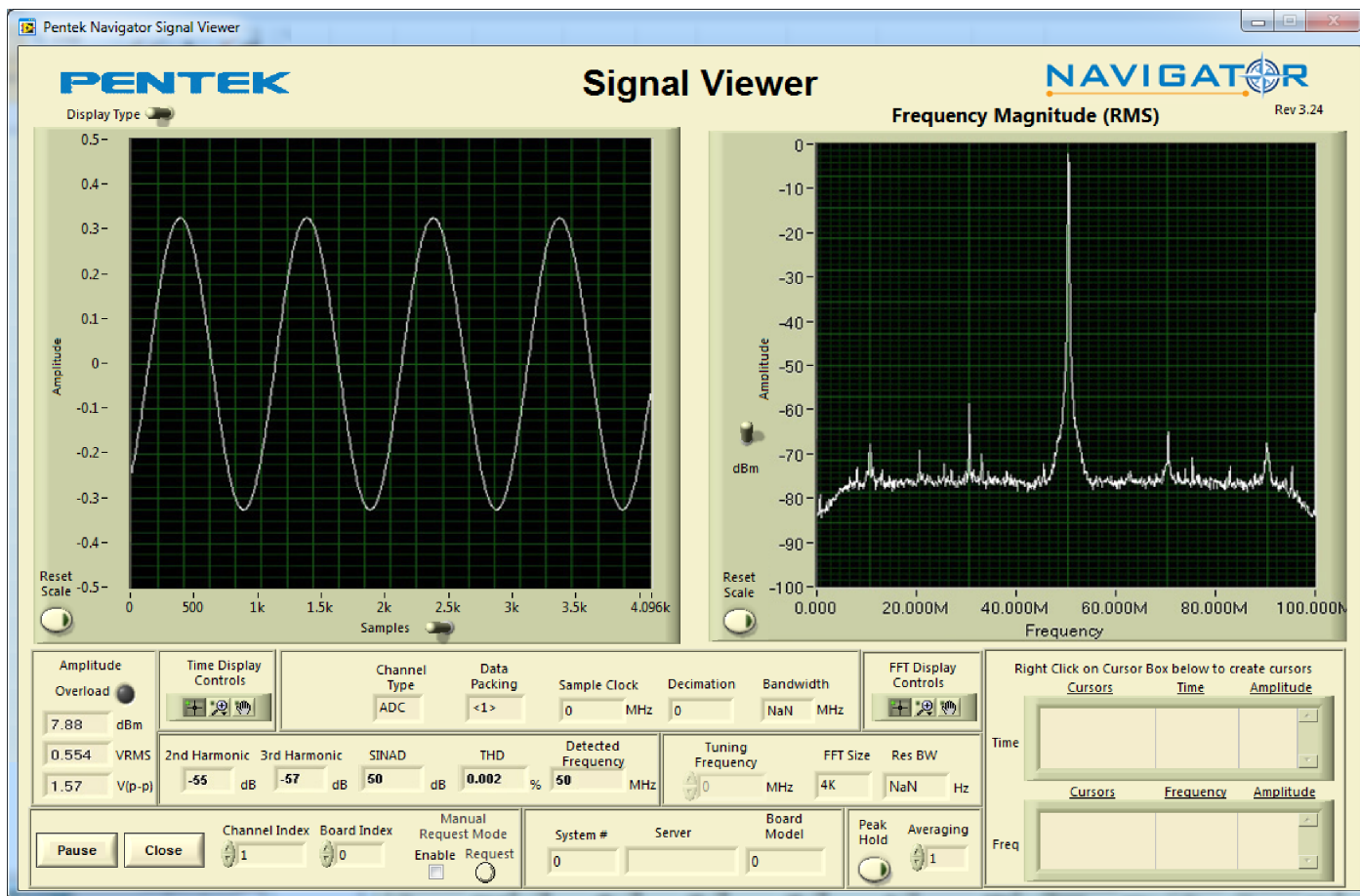
The **Navigator Board Support Package (BSP)** provides software support for Pentek boards. It enables operational control of all hardware functions on the board and IP functions in the FPGA.

The BSP structure is designed to complement the functions of the FDK by maintaining a one-to-one relationship between FDK and BSP components. For each IP block found in the FDK library, a matching software module can be found in the BSP. This organization simplifies the creation and editing of software to support new IP functions and modifications to existing IP cores.



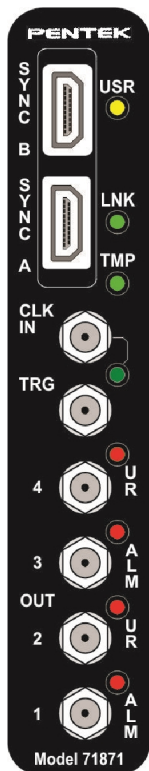
Because all Pentek boards are shipped with a full suite of built-in IP functions and numerous software examples, new applications can be developed by building on the provided software examples or built entirely new with the BSP extensive libraries. All BSP libraries are provided as C-language source for full access and code transparency.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.



Front Panel Connections

The front panel includes six SSMC coaxial connectors for input/output of timing and analog signals, and two 19-pin Sync Bus input connectors. The front panel also includes eight LED indicators.



- **Sync Bus Connector:** The 19-pin μ Sync front panel connector, labeled **SYNCA** and **SYNCA** provide sync, and gate inputs for DAC timing control.
- **User LED:** The green **USR** LED is for user applications.
- **Link LED:** The green **LNK** LED illuminates when a valid link has been established over the PCIe interface.
- **Over Temperature LED:** The red **TMP** LED illuminates when an over-temperature or over-voltage condition is indicated by any of the temperature/voltage sensors on the PCB.
- **Clock Input Connector:** One SSMC coaxial connector, labeled **CLK IN**, for input of an external sample or reference clock.
- **Clock LED:** The green **CLK** LED illuminates when a valid sample clock signal is detected. If the LED is not illuminated, no clock has been detected and no data from the input stream can be processed.
- **Trigger Input Connector:** One SSMC coaxial connector, labeled **TRIG** for input of an external gate or trigger TTL signal.
- **Analog Output Connectors:** Four SSMC coaxial connectors, labeled **OUT 1**, **2**, **3**, and **4**: one for each DAC3484 output channel.
- **Analog Input Connectors:** Two SSMC coaxial connectors, labeled **IN 1** and **IN 2**: one for each ADC input channel.
- **DAC Underrun LEDs:** Two red underrun **UR** LEDs for each DAC3484 device. This LED illuminates when the DAC5688 FIFO is out of data.

- **DAC Alarm LEDs:** Two red **ALM** alarm LEDs for each DAC3484 device. The **ALM** LED next to **OUT 1** is for DAC 3484 A; the **ALM** LED next to **OUT 3** is for DAC3484 B. Each LED illuminates when the associated DAC3484 Alarm output is active.

Specifications

D/A Converters

Type: Texas Instruments DAC3484

Input Data Rate: 312.5 MHz max.

Output Bandwidth: 250 MHz max.

Output Sampling Rate: 1.25 GHz max. with interpolation

Interpolation: 2x, 4x, 8x or 16

Resolution: 16 bits

Digital Interpolator Core

Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Total Interpolation Range (D/A and interpolator core combined)

2x to 1,048,576x

Front Panel Analog Signal Outputs

Output: Transformer-coupled, front panel female SSMC connectors

Transformer: Coil Craft WBC4-6TLB

Full Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources

On-board clock synthesizer generates D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 3, 4, 6, 8, or 16, independently for the D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

19-pin μ Sync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input**Type:** Front panel female SSMC connector, LVTTTL**Function:** Programmable functions include: trigger, gate, sync and PPS**Field Programmable Gate Array****Standard:** Xilinx Kintex UltraScale XCKU035-2**Option -084:** Xilinx Kintex UltraScale XCKU060-2**Option -087:** Xilinx Kintex UltraScale XCKU115-2**Custom I/O****Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA**Option -105:** Provides one 8X gigabit link between the FPGA and XMC P16 connector to support serial protocols.**Memory****Type:** DDR4 SDRAM**Size:** 5 GB**Speed:** 1200 MHz (2400 MHz DDR)**PCI-Express Interface****PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8**Environmental****Standard: L0 (air cooled)**

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction-cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Physical**Dimensions:** Single XMC module

Depth: 149.10 mm (5.87 in)

Height: 73.91 mm (2.91 in)

Weight: Approximately 14 oz (400 grams)**Ordering Information**

Model	Description
71871	4-Channel 1.25 GHz D/A with DUC and Extended Interpolation, and Kintex UltraScale FPGA - XMC

Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P14 connector
-105	Gigabit serial FPGA I/O through P16 connector
-702	Air-cooled, Level 2
-713	Conduction-cooled, Level 3
-730	2-slot heat sink
Contact Pentek for compatible Option combinations, complete specifications of rugged and conduction-cooled versions. Storage and General Options may change, contact Pentek for latest information.	

Accessory Products

Model	Description
2171	Cable Kit: SSMC to SMA
7192	High-Speed Synchronizer and Distribution Board - PMC/XMC Model
9192	Rackmount High-Speed System Synchronizer Unit

SPARK Development Systems

The Pentek **SPARK® systems** are fully-integrated development systems for Pentek software radio, data acquisition, and I/O boards. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

The following SPARK systems are available for Pentek's Cobalt®, Onyx®, and Jade® boards: PCIe (Model 8266), 3U OpenVPX (Model 8267) and 6U OpenVPX (Model 8264). For Flexor boards, SPARK systems are available in PCIe (Model 8266) and 3U VPX (Model 8267).



Pricing and Availability

To learn more about our products or to discuss your specific application please contact [your local representative](#) or Pentek directly:

Pentek, Inc.
One Park Way
Upper Saddle River, NJ 07458 USA
Tel: +1 (201) 818-5900
Email: sales@pentek.com

Lifetime Applications Support

Pentek offers the worldwide military embedded computing community shorter development time, reliable, rugged solutions for a variety of environments, reduced costs, mature software development tools and **free**, lifetime support that our customers can depend on: phone and email access to engineering staff as well as software updates. Take advantage of Pentek's expertise in delivering high-performance radar, communications, SIGINT, and data acquisition MIL-Aero solutions worldwide for over 30 years.