Cover removed to show Model 6001 QuartzXM eXpress Module

Features

- Supports Xilinx Zynq UltraScale+ RFSoC FPGAs
- 16 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3)
- 40 GigE Interface
- Optional VITA 67.3D optical interface for backplane gigabit serial communication
- Dual 100 GigE UDP interface
- Compatible with several VITA standards including: *VITA 46, VITA 48, VITA 67.3D and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available
- Unique QuartzXM eXpress Module enables migration to other form factors

General Information

The Quartz Model 5550 is a high-performance, SOSA aligned 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The Model 5550 brings RFSoC performance to 3U VPX with a complete system on a board.

Complementing the RFSoC's on-chip resources are the 5550's sophisticated clocking section for single board and multi-board synchronization, a low-noise front end for RF input and output, 16 GBytes of DDR4, a PCIe interface, a 40 GigE interface, a gigabit serial optical interface capable of supporting dual 100 GigE connections and general purpose serial and parallel signal paths to the FPGA.

Board Architecture

The 5550 board design places the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Pentek developed IP and software functions utilize this architecture to provide data capture, timing, and interface solutions for many of the most common application requirements.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits (FDK) include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 5550's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 5550 either from applications running locally on the ARMs, or using the Navigator API, control and command from remote system computers.

A/D Converter Stage

The front end accepts analog IF or RF inputs on eight coax connectors located within a VITA 67.3D connector. These inputs are transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.
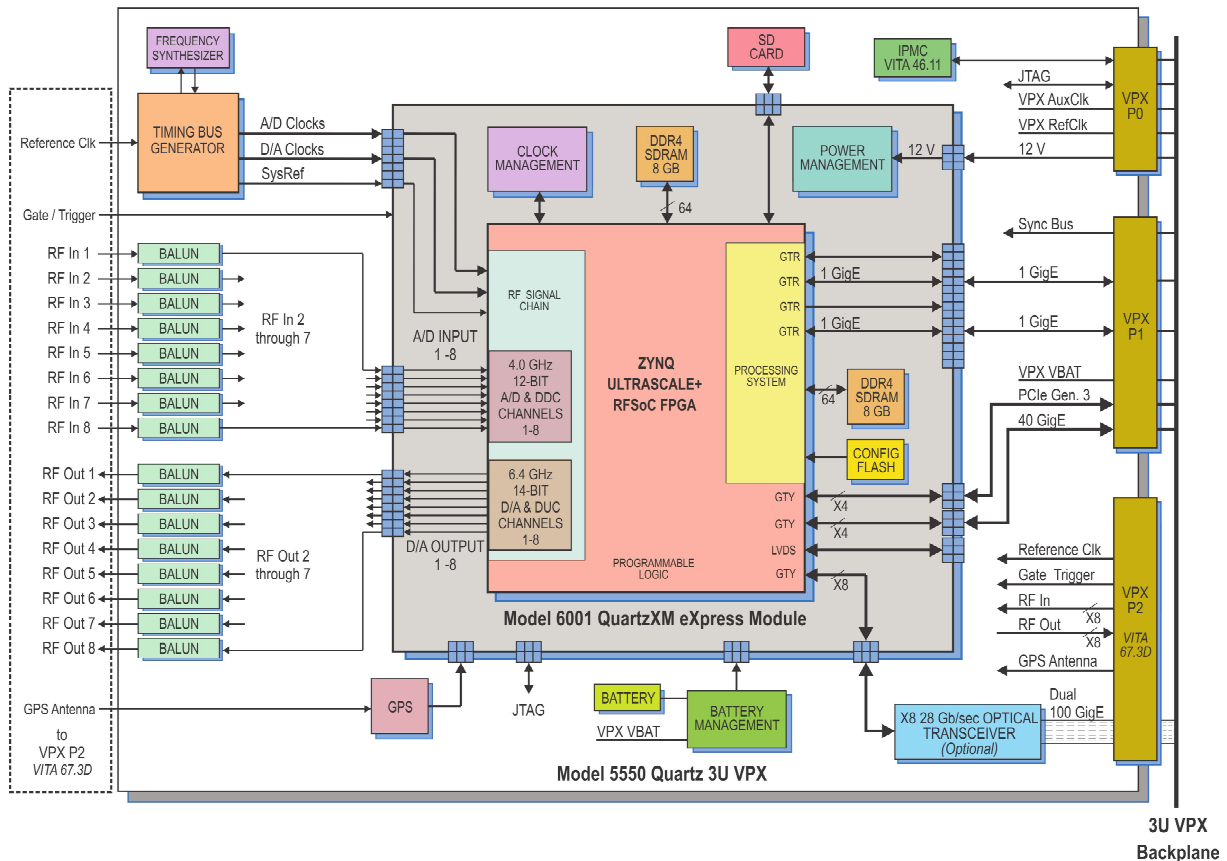
D/A Converter Stage

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x , 4x and 8x. Each D/A output is transformer coupled to a coax connection located within a VITA 67.3D connector.

Clocking and Synchronization

An on-board timing bus generator uses a programmable frequency synthesizer to generate the sample clock and all required timing signals. the on-board sample clock can also be locked to a reference clock received through one of the VITA 67.3D connectors. A multifunction gate/trigger input is also available on one of the VITA 67.3D connectors for external control of data acquisition and playback.

For larger systems requiring multi-board synchronization, a multi-signal sync bus interface is provided on the VPX P1 connector. These signals include the sample clock and all required complemen-

FREQUENCY SYNTHESIZER

SD CARD

IPMC VITA 46.11

JTAG

VPX AuxClk

VPX RefClk

12 V

VPX P0

Reference Clk

TIMING BUS GENERATOR

A/D Clocks

D/A Clocks

SysRef

CLOCK MANAGEMENT

DDR4 SDRAM 8 GB

POWER MANAGEMENT

12 V

12 V

Gate / Trigger

Sync Bus

RF In 1
RF In 2
RF In 3
RF In 4
RF In 5
RF In 6
RF In 7
RF In 8

BALUN

RF In 2 through 7

A/D INPUT 1 -8

RF SIGNAL CHAIN

4.0 GHz 12-BIT A/D & DDC CHANNELS 1-8

ZYNQ ULTRASCALE+ RFSoC FPGA

PROCESSING SYSTEM

GTR
GTR
GTR
GTR

1 GigE

1 GigE

1 GigE

1 GigE

VPX P1

VPX VBAT

PCIe Gen. 3

40 GigE

64

DDR4 SDRAM 8 GB

RF Out 1
RF Out 2
RF Out 3
RF Out 4
RF Out 5
RF Out 6
RF Out 7
RF Out 8

BALUN

RF Out 2 through 7

D/A OUTPUT 1 -8

6.4 GHz 14-BIT D/A & DUC CHANNELS 1-8

PROGRAMMABLE LOGIC

CONFIG FLASH

GTY

GTY

LVDS

GTY

X4

X4

X8

Reference Clk

Gate Trigger

RF In

RF Out

GPS Antenna

VPX P2

VITA 67.3D

X8

X8

Model 6001 QuartzXM eXpress Module

GPS Antenna

to VPX P2 VITA 67.3D

GPS

JTAG

BATTERY

VPX VBAT

BATTERY MANAGEMENT

X8 28 Gb/sec OPTICAL TRANSCEIVER *(Optional)*

Dual 100 GigE

Model 5550 Quartz 3U VPX

3U VPX Backplane

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tary timing signals to provide single sample accurate synchronization across multiple boards. The Model 5903 High-Speed Synchronizer and Distribution 3U VPX Board is available as a programmable clocking and sync source for these high channel count Quartz systems.

Expandable I/O

The Model 5550 supports eight 28 Gb/sec full duplex optical lanes to one of the VITA 67.3D connectors. With the built-in 100 GigE UDP interface or installation of a user provided serial protocol, this optical interface enables a high speed gigabit data streaming path between boards.

Memory Resources

The 5550 architecture supports 8 GBytes of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Pentek supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

An additional 8 GByte bank of DDR4 SDRAM is available to the Processing System as program memory and storage.

PCI Express Interface

The Model 5550 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

40 GigE Interface

The Model 5550 includes a 40 GigE interface for control and data transfers. This interface is independent of both the PCIe and the optical 100 GigE interfaces.

GPS

An optional GPS receiver provides time and position information to the FPGA and ARM processors. This information can be used for precise data tagging. The GPS provides a 1 PPS and 10 MHz reference clock to the FPGA.


Optimized IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Pentek helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications. For each example that follows the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Pentek Navigator IP library or for adding custom IP.

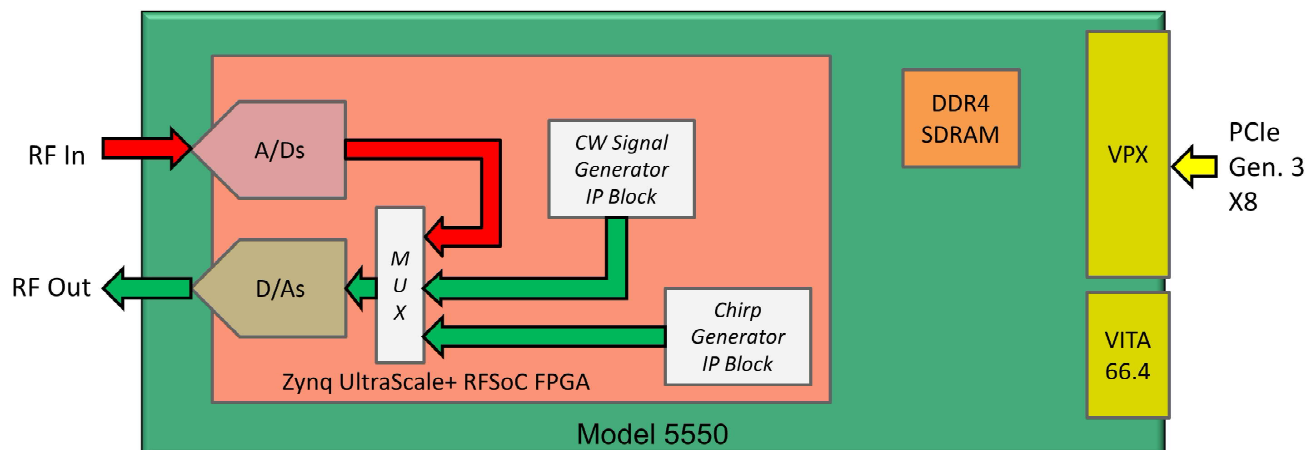## Example Application 1 - High Bandwidth Data Streaming

The RFSoC's eight 4 GSPS A/Ds are capable of producing an aggregate data rate of 64 GBytes/sec when all channels are enabled. While capturing this much raw data is not feasible, the A/Ds built-in digital down converters can reduce this data throughput in many applications to a rate reasonable for the data streaming and storage components downstream in the system.

In some applications capturing the raw, full bandwidth data is crucial. The 5550's dual 100 GigE UDP engine provides a high bandwidth path for moving data off of the board. Along with the built-in data acquisition IP, the 5550 can stream two full bandwidth A/D data streams over optical cable to a downstream storage or processing subsystem.
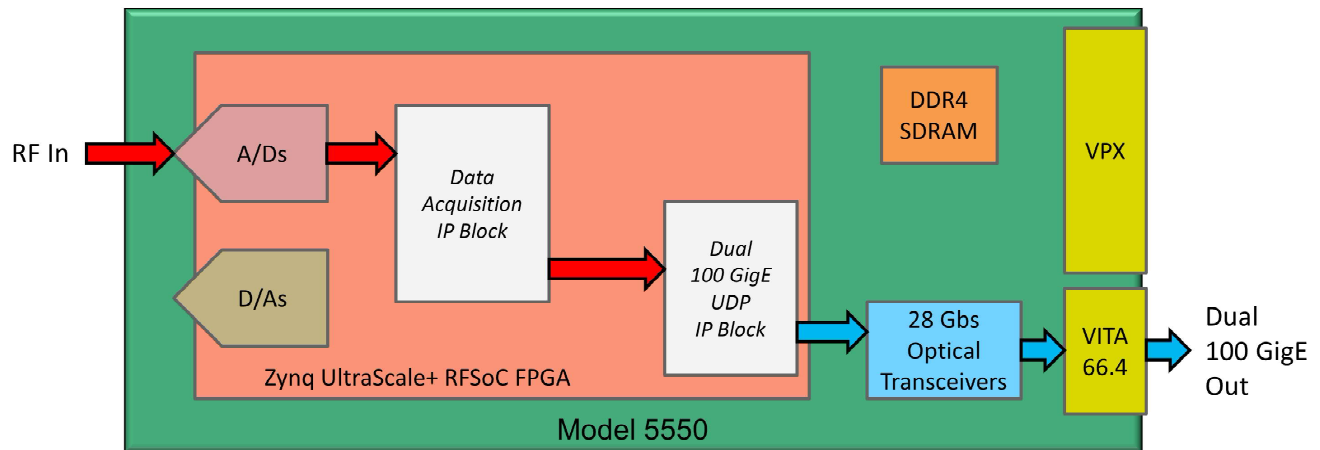

Example Application 2 - Waveform Generator

The 5550's IP supports multiple D/A signal source options. A simple loopback path allows samples received by the A/Ds to be output through the D/As. A CW signal generator produces a sine output with programmable frequency. A chirp generator, ideal for radar applications, outputs sweep signals with programmable frequency, ramp, phase offset, gain offset and length. The generators also include flexible trigger options with both internal and external triggering.

Example Application 3 - Multi-mode Data Acquisition System

In some applications multiple data acquisition modes may need to be operated at the same time. A required dataflow could be full bandwidth streaming of a single A/D channel over 100 GigE to a data recorder while another channel of A/D data is stored as snapshots in the boards DDR4 SDRAM and read by the ARM processor while yet other A/D channels are down converted using the A/Ds' built-in DDCs and streamed over PCIe. The 5550 provides these modes with built-in IP supporting complex data streaming scenarios without the need for creating custom IP.
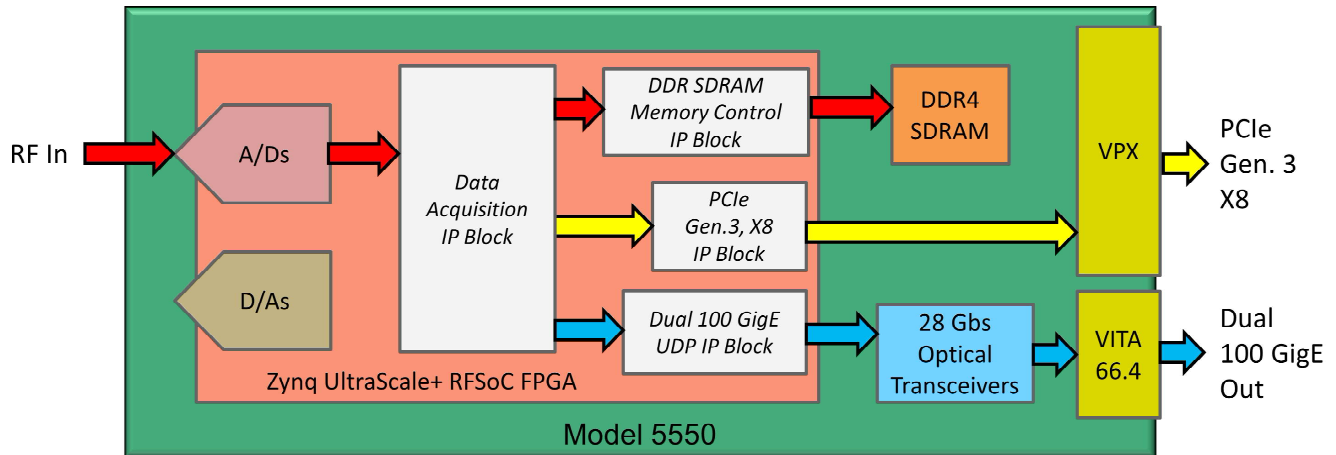

Flexible Modular Design

While the Model 5550 follows the form factor of a standard 3U OpenVPX board, the unique modular design of Pentek's Model 6001 QuartzXM eXpress Module provides the flexibility to deploy this solution in many different situations. The heart of the QuartzXM is a system on module containing all of the key components including the RFSoC FPGA, DDR4 SDRAM, and power and clock management.

In the case of the 5550 the QuartzXM is mounted on a 3U OpenVPX carrier which complements the design with a timing bus generator, analog signal conditioning, a GPS receiver and an 8x 28 Gbps optical transceiver. As a module and carrier board set, the 5550 becomes a complete, ready to deploy 3U OpenVPX solution available for a range of operating environments from commercial to rugged and conduction cooled.

The Model 6001 QuartzXM can also be mounted on other carriers available from Pentek to support standard form factors, or for applications that require a non-standard footprint, Pentek supports the module with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best in class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.
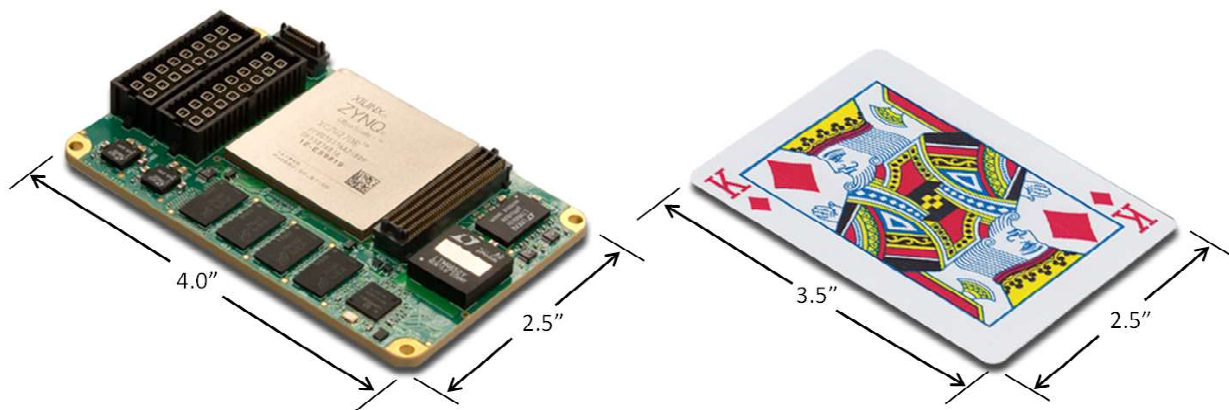
Model 6001 QuartzXM eXpress Module

Specifications - Model 5550

Field Programmable Gate Array
  Type: (standard) Xilinx Zynq UltraScale+ RFSoC XCZU27DR
    Option -028: Xilinx Zynq UltraScale+ RFSoC XCZU28DR
  Speed: (standard) -1 speed grade
    Option -002: -2 speed grade

RFSoC RF Signal Chain
  Analog Inputs:
    Quantity: 8
    Connector: VITA 67.3D
    Input Type: Transformer-coupled
    Transformer Type: Mini-Circuits TCM1-83X+
    Full Scale Input: +4 dBm into 50 ohms (includes matching network)
    3 dB Passband: 10 MHz to 4000 MHz
  A/D Converters:
    Quantity: 8
    Sampling Rate: 4.0 GHz
    Resolution: 12 bits
  Digital Downconverters:
    Quantity: 1 per A/D
    Decimation Range: 1x, 2x, 4x and 8x
    LO Tuning Freq. Resolution: 48 bits, 0 to f_s
    Filter: 80% pass band, 89 dB stop-band attenuation
  Analog Outputs:
    Quantity: 8
    Connector: VITA 67.3D
    Input Type: Transformer-coupled
    Transformer Type: Mini-Circuits TCM1-83X+
    Full Scale Output: +4 dBm into 50 ohms
    3 dB Passband: 10 MHz to 4000 MHz
  D/A Converters:
    Quantity: 8
    Sampling Rate: 6.4 GHz
    Resolution: 14 bits
  Digital Upconverters:
    Quantity: 1 per D/A
    Interpolation Range: 1x, 2x, 4x and 8x
    LO Tuning Freq. Resolution: 48 bits
    Filter: 80% pass band, 89 dB stop-band attenuation
  Sample Clock Source: On-board programmable clock source
  Reference Sync and Gate/Trigger: Received on VITA 67.3D connector

RFSoC RF Processing System
  ARM Cortex-A53:
    Quantity: 4
    Speed: 1.5 GHz
  ARM Cortex-R5:
    Quantity: 2
    Speed: 600 MHz

Custom FPGA I/O
  Optical (Option 110): 8X full duplex lanes @ 28 Gb/sec on VITA 67.3D connector

Memory
  Processing System:
    Type: DDR4 SDRAM
    Size: 8 GBytes;
    Speed: 1200 MHz (2400 MHz DDR)
  Programmable Logic:
    Type: DDR4 SDRAM
    Size: 8 GBytes;
    Speed: 1200 MHz (2400 MHz DDR)
    FPGA Configuration FLASH: 2x 1 Gbit QSPI

PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
  Level L3 (conduction cooled)
    Operating Temp: –40 to 70 C
    Storage Temp: –50 to 100 C
    Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5550 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:
  SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n

Model 8257

The Model 8257 is a 1-Slot 3U VPX chassis. Offered as a convenient, low cost solution for hosting the 5550, it includes power and cooling to match the 5550's requirements in a portable desk top package.
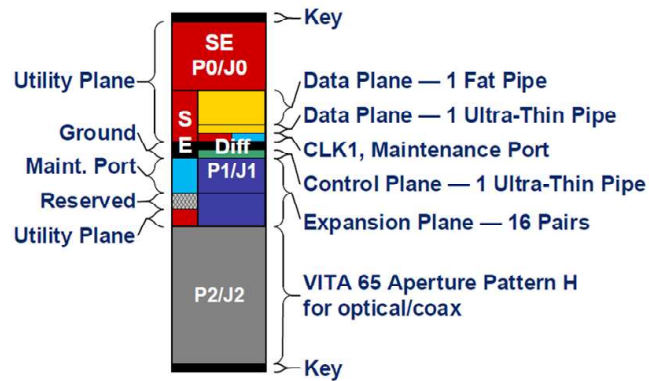
Ordering Information

Model	Description
5550	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - SOSA Aligned 3U VPX

Options:

-002	-2 FPGA speed grade, -1 standard
-028	XCZU28DR FPGA, XCZU27DR standard
-108	VITA 67.3D 8X optical interface
-180	GPS support

Model	Description
8257	1-Slot 3U VPX Development Chassis See 8257 Datasheet for Options