The New Wave DV V1153 Rugged XMC FPGA Card: Combining Customizable High-Speed Interfaces with FPGA Coprocessing

Built for harsh environments, high performance, and sensitive budgets, the new FPGA-based XMC meets VITA 47 rugged specs and offers custom or pre-configured high-speed serial interfaces along with powerful FPGA coprocessing to speed up and simplify system development.

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The new V1153 rugged VITA 42 XMC interface and FPGA processor card introduced by New Wave Design & Verification (New Wave DV) offers users a unique combination of high-speed interfacing modes and powerful application coprocessing capabilities. The V1153 provides multiple high-speed serial interfaces to the host, allowing communication over PCI Express (PCIe), Ethernet, and other protocols. New Wave DV's V1153 XMC offers system designers a combination of capabilities to optimize high-speed interfacing, networking, and processing solutions in applications such as radar, signal intelligence, video, electronic warfare, medical imaging, and embedded telecommunications. All interfaces, protocol offloads, and host interface functions are under control of the FPGA, resulting in vast port flexibility and protocol configuration with options for user-provided algorithms executed by the on-board FPGA.

Technical Features

The V1153 is a VITA 42 compliant XMC, meeting the VITA 20 dimensions for conduction cooling, and meets the VITA 47 ECC4 ruggedization specifications for shock, vibration, and operating temperature range of -40° C to +85° C. Pluggable into a 3U or 6U VPX chassis, data transfer can be over a PCIe connection up to PCIe Gen3 x 16. Other connectivity options are available, such as running Ethernet (or another protocol) to/from the front panel or back panel connectors, providing almost unlimited flexibility. This allows the V1153 to mount to a wide range of existing VPX single-board computers and carriers. The combined solution fits into a single slot of a VPX chassis, providing a huge interface and processing offload capability to the system without taking an extra chassis slot.

The V1153 offers up to twelve 1Gbs to 25Gbs optical ports via a front panel multichannel push-on (MPO) connector or a choice of VITA 66.1 or VITA 66.4 optical backplane connectors. In all cases, the V1153 features the Samtec FireFly™ Micro Flyover System™ which can use high-performance optical or copper cable assemblies with the same connector. A 16-port electrical backplane may also be utilized, configurable from 1Gbs up to 16Gbs. New Wave DV supports a variety of pre-configured network protocols including Ethernet, Fibre Channel, sFPDP, ARINC 818, and Aurora. In addition, New Wave DV can supply options for custom high-speed serial protocols and user-developed IP solutions.

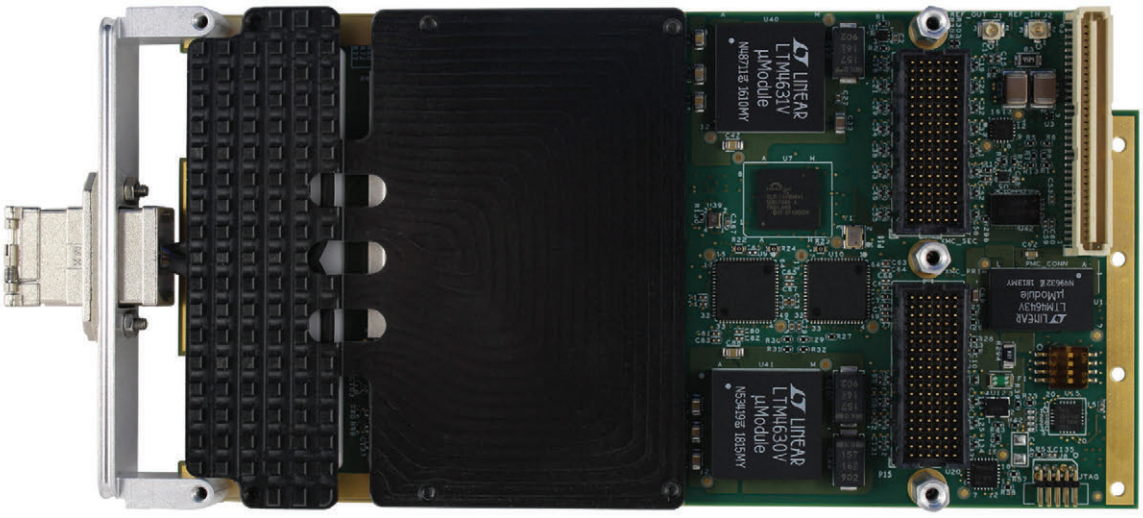


Figure 1: The V1153 is a rugged XMC FPGA card for high-speed interface and coprocessing solutions. It offers 4 to 12 optical port options (front panel or backplane) as well as 1-16Gbs electrical backplane ports.

Table 1: Available V1153 optical and electrical configuration options. For example, 4 optical ports can be configured into a 100Gbs Ethernet interface, or can be used as four 25Gbs or 10Gbs interfaces.

V1153 Interface Configuration Options					
Protocol	**Optical**			**Electrical**	
	4-Port	***8-Port***	***12-Port***	***Pn5***	***Pn6***
100G Ethernet	1	2	N/A	N/A	N/A
40G Ethernet	1	2	3	2	2
25G Ethernet	4	8	N/A	N/A	N/A
10G Ethernet	4	8	12	8	8
1G Ethernet	4	8	12	8	8
1/2/4/8/16Gbs Fibre Channel	4	8	12	8	8
1/2/2.5/4.25/5Gbs sFPDP	4	8	12	8	8
ARINC 818 (Up to 16Gbs)	4	8	12	8	8
Aurora (Up to 16Gbs)	4	8	12	8	8
PCIe (Gen3 x 8)	N/A	N/A	N/A	1	1

Configuration Options

The large optical/electrical port count can be configured by pre-loaded FPGA IP or customer designs to support a variety of protocols. Some protocol interfaces consist of multiple underlying physical ports, such as 40Gbs and 100Gbs Ethernet. In those cases, the ports are bonded together to provide the desired physical network configuration. Table 1 shows the resultant network interface counts used to support the various V1153 configuration options.

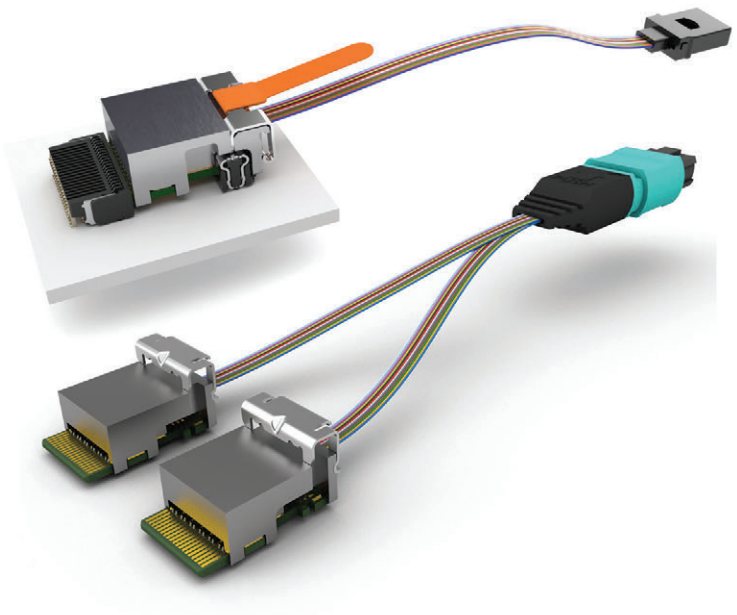


Figure 2: Two Samtec FireFly™ optical connection options to standard connectors: (A) a MPO connection and (B) a VITA 66.4 connection. Cables can be provided for desired cable lengths.

The V1153 is designed to meet a number of optical and electrical interface requirements. To address these needs, an array of optical port options are available, as well as electrical backplane connections providing up to 16 electrical ports. While electrical interfaces can be used simultaneously with the optical ports, only one optical style connector (MPO faceplate or VITA 66 backplane) can be used at a time. For backplane configurations, MT-terminated optical cable(s) are provided for mating with the VITA 66 connector on the customer carrier card (Figure 2). New Wave DV also welcomes requests for custom IO configurations.

Built For Programmability

The V1153 card can be ordered pre-configured with user-desired interface cores as a turnkey unit, ready to use out-of-the-box. The availability of pre-loaded interface cores provides a powerful set of options to end-users. Pre-configured IP cores allow system designers to focus on value-added development instead of recreating standard interfaces. Available interface cores on the V1153 are currently: Ethernet, Fibre Channel, sFPDP, ARINC 818, and Aurora.

Another benefit of the V1153 is the onboard FPGA, which can serve as a powerful application coprocessor. The FPGA can host all or part of a user's application and/or algorithms, such as interface protocol removal from streaming data, compression, encryption/decryption, or image processing. Access to the FPGA is provided on the V1153 even when a New Wave-provided interface core is present. This allows for designers to co-locate the interface and data processing aspects of the design, reducing latency and overhead of the system. The following FPGAs are available on the V1153: Xilinx Virtex® UltraScale+™ (VU3P) and Xilinx Kintex® UltraScale™ (KU095).

The V1153 is available without pre-configured IP from New Wave. In this use case, the customer provides the entire FPGA design. New Wave DV provides the necessary FPGA pinouts and card architecture documentation to enable design success by the customer.

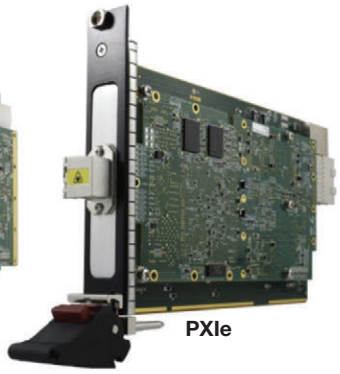
The V1153 provides both on-board and backplane JTAG

ports as well as an RS-232 port to enable development using industry standard design tools and the provided development framework. This framework provides a hardware abstraction layer that communicates with the board level infrastructure. There are also pre-designed elements including PCIe controllers, network ports, and DDR memory. This allows the user to focus on the core functionality and not the mechanics of moving data between the host and network.

Form Factor Compatibility

In addition to different interface standards and FPGA IP configuration options, the V1153 offers numerous form factor offerings. The V1153 VITA 42 XMC card, dimensionally compliant with VITA 20 conduction cooling, has been designed and tested to operate with a variety of processor and carrier cards in various form-factors. Common form-factors supported by the V1153 include (but are not limited to): 3U VPX (air and conduction cooled), 6U VPX (air and conduction cooled), VME (air and conduction cooled), PXIe, PCIe, and CompactPCI. This form-factor versatility, combined with the innate power of the V1153, makes it perfect for test and embedded applications of all kinds. Today, the V1153 is reliably being used in exhaustive lab/test environments as well as in turnkey solutions in a variety of demanding embedded applications.


PCIe


PXIe


VPX
(backplane config)


VPX
(front panel IO)

The New Wave IP Suite

The optionally pre-loaded IP cores include Ethernet, Fibre Channel, sFPDP, ARINC 818, and Aurora. Each New Wave DV IP core has a range of standard and protocol-specific features, dependent on the selected protocol. The following table lists available cores and their capabilities:

Protocol	Unique Specs	Configurable # of Ports	AXI-Based Host Interface	Hardware DMA Engine
Fibre Channel ULP (Upper Layer Protocol) (FC-ULP)	FC-RDMA and FC-AV protocol offload Configurable compatibility modes for various FC specifications LUN and Container processing in hardware	✓	✓	✓
Fibre Channel ASM (Anonymous Subscriber Messaging) (FC-ASM)	FC-ASM protocol offload Hardware-based label verification Provides label-to-host memory buffer-mapping	✓	✓	✓
sFPDP (Serial Front Panel Data Port)	Complies with VITA 17.1-2015 Software-Configurable 1/2/2.5/4.25/5Gbs Rates Configurable Sync Frames	✓	✓	✓
ARINC 818	Run-time configurable ARINC 818 ICD parameters Software-Configurable 1/2/3/4/8Gbs rates Video Frame Buffers	✓	✓	✓
Ethernet	FPGA-based PCAP encapsulation Packet-coalesced DMA controller for reduced CPU utilization VITA 49 support	✓	✓	✓
Aurora	Configurable rate and channel bonding support FPGA-based PCAP encapsulation Packet-coalesced DMA controller for reduced CPU utilization	✓	✓	✓

Each core is designed to be pre-loaded in the FPGA (optionally) and provide the complete design from software API to the physical network interface. Each loadable core comes with test-benches and example code, making design integration a straightforward task.

FPGA Power to Process

The FPGA controls the optical and electrical interfaces as well as the PCIe connection. Using installed firmware, the FPGA can control the interfaces, transmit/receive the network traffic, add/remove the protocol stack, and move payload data across PCIe from/to a host processor formatted for the application at hand. For example, Ethernet has several layers—IP, UDP, etc.—that are removed before the data is ready for use by the application. These layers can be removed in-line at wire speed by the FPGA as the data is received from the network connection. Conversely for transmit, the core automatically formats the outgoing data with the needed network layers. Assigning traffic handling, data formatting, and preliminary steps of the application to the FPGA is a significant relief for the host processor.

The powerful FPGA on this mezzanine board may be used as an application coprocessor. The V1153 fits with the processor board in a single backplane slot for application acceleration. As FPGAs are especially useful for parallel processing, a user can put all or some portion of, for example, a radar processing application, onto the V1153. The FPGA can perform signal processing, spectral analysis, and data transforms. Integrating these user algorithms is made even easier by the development framework offered by New Wave DV using industry-standard tools. Customers can add their own algorithms and "secret sauce" to run under the FPGA using the development framework offered by New Wave DV.

This development framework is compatible with standard FPGA development tools from major vendors and comes with a hardware abstraction layer, called the interface wrapper, along with a user-development region ('sandbox') where developers can design and develop their own code. The abstraction layer offers a user-application interface to all the FPGA and board-level resources needed for high performance data interfacing and processing.

The framework also has an assortment of software APIs, kernel drivers, and software examples to help programmers develop applications that communicate seamlessly with the development framework. So, when the data is fed into the user sandbox, it has already been separated from

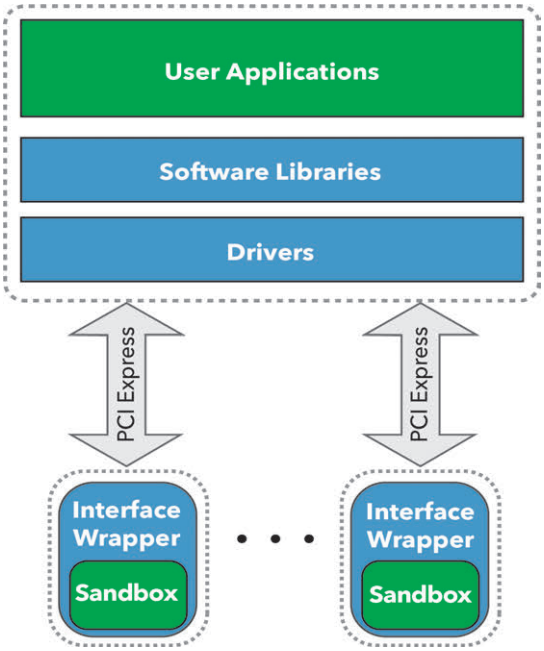


Figure 3: The development framework offers a hardware abstraction layer to all the interfaces required for a FPGA in the form of the interface wrapper. The sandbox region allows developers to create, test, and evaluate both the example code provided, as well as their own custom code.

the protocols and can be processed by the user's own algorithms. On the other side of the sandbox is the DMA controller and the PCIe interface to transfer the partially processed data to the host processor for further processing and use by the application. The V1153's Gen3 PCIe interface allows it to operate with almost any host system.

Summary

The V1153 was built for harsh environments, high performance, and sensitive budgets. Offering a broad selection of network formats and interface configurations, it allows system developers to incorporate high-bandwidth interface solutions with high port density, rugged operation, and high processing power for a wide range of uses such as radar, signal intelligence, video, electronic warfare, medical imaging, and embedded telecommunications. It offers this selection of solutions while also supplying high-power FPGA processing. The V1153 provides a broad platform for the creation of rugged, reliable, and powerful embedded interface solutions that will meet demanding performance, environmental, and cost requirements.

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