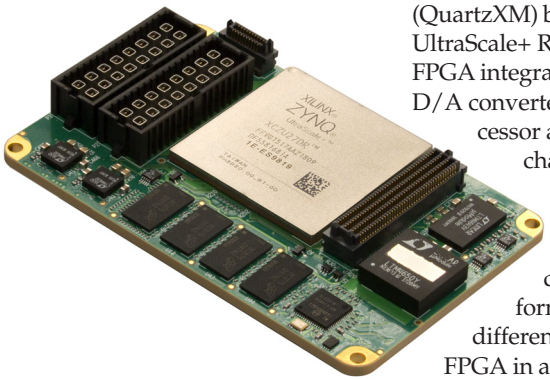
New!

Model 6001

8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - QuartzXM



2.5″ x 4.0″ Quartz Express Module

QUARTZ

NAVIGATOR Design Suite

Features

- Unique QuartzXM eXpress Module enables deployment in custom form factors
- Supports Xilinx Zynq UltraScale+ RFSoC FPGAs
- 18 GB of DDR4 SDRAM
- LVDS connections to the Zynq UltraScale+ FPGA for custom I/O
- GTY connections for gigabit serial communication
- Ruggedized and conduction-cooled versions available
- Includes a complete suite of IP functions and example applications

General Information

The Quartz Model 6001 is a high-performance Quartz eXpress Module (QuartzXM) based on the Xilinx Zynq UltraScale+ RFSoC FPGA. The RFSoC FPGA integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multi-channel data conversion and processing solution on a single chip.

The Model 6001 has been designed to bring RFSoC performance to a wide range of different applications by offering the FPGA in a small system on module solution measuring only 2.5 by 4 inches. In addition to the RFSoC FPGA, the 6001 includes all of the support circuitry needed to maximize the performance of the RFSoC.

The 6001 is available on standard form factor carriers. The Pentek Model 5950 delivers the 6001 as a 3U OpenVPX Commercial Off The Shelf (COTS) board available in air cooled and fulled rugged and conduction cooled versions. In many applications, the 3U VPX standard form factor carrier can provide a final, deployable turn-key solution.

In situations where only a custom form factor will satisfy the application requirements, Pentek supports the 6001 with a design kit for users to engineer and build their own custom carrier. As a complete and tested module, the QuartzXM encapsulates best in class electrical and mechanical design, eliminating some of the most challenging aspects of embedded circuit design and allowing the user to focus on the application specific carrier design.

Board Architecture

The 6001 board design positions the RFSoC as the cornerstone of the architecture. All control and data paths are accessible by the RFSoC's programmable logic and processing system. A full suite of Pentek developed IP and software functions utilize this architecture to provide data capture, generation and processing solutions for many of the most common application requirements. For many applications the Model 6001 can be used with simply the built-in functions, requiring no FPGA IP to be developed.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits (FDK) include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado IP Integrator. In addition to the IP Integrator block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

The Navigator Board Support Package (BSP), the companion product to the Navigator FDK, provides a complete C-callable library for control of the 6001's hardware and IP. The Navigator FDK and BSP libraries mirror each other where each IP function is controlled by a matching software function, simplifying the job of keeping IP and software development synchronized.

The Navigator BSP includes support for Xilinx's PetaLinux running on the ARM Cortex-A53 processors. When running under PetaLinux, the Navigator BSP libraries enable complete control of the 6001 either from applications running locally on the ARMs, or using the Navigator API, control and command from remote system computers.

A/D Converter Stage

The 6001 accepts analog IF or RF inputs from the carrier board on a multi-channel connector, delivering the inputs as differential pairs into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4 GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

In addition to the A/D's built-in decimation, an additional stage of IP based decimation provides another 16x stage of data reduction, ideal for applications that need to stream data from all eight A/Ds.

D/A Converter Stage

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4 GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x , 4x and 8x. The individual D/A outputs are delivered to the carrier board through a multi-channel connector as differential pairs.

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When the 6001 QuartzXM is installed on Pentek's 3U Open VPX carrier as the Model 5950, both the RF inputs and outputs are transformer coupled to front panel MMCX connectors. For applications that require special analog processing or connectorization, the 6001 can be mounted on a custom designed carrier to satisfy the specific application requirements.

Clocking and Synchronization

The 6001 accepts all of the clock signals required by the RFSoC through a multi-signal connector from the carrier. In addition, the 6001 design includes a clock management section for distributing the clock and synchronization signals throughout the module.

Expandable I/O

The 6001 provides an interface to all of the digital signals needed by the RFSoC's processing system and programmable logic sections through a high speed connector to the carrier. The RFSoC's GTY high-speed gigabit serial interfaces are supported by connectors capable of delivering 28 Gb/sec, needed for protocols like 100GigE.

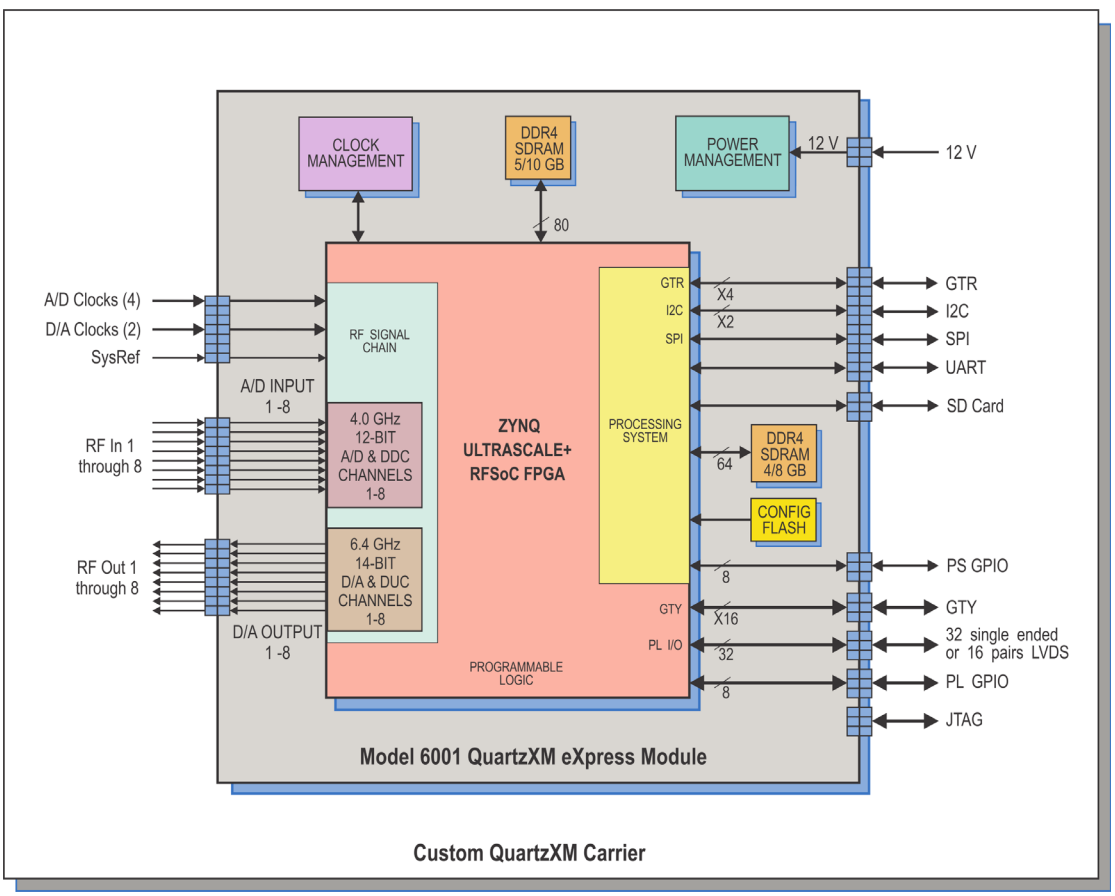
Power Supplies and Sequencing

The RFSoC FPGA requires nine different and separate power supplies. In addition, other peripheral circuits needed by the RFSoC require separate supplies. The 6001 includes thirteen different on-board power supplies to support the RFSoC and associated circuitry. Because the supply complexity and sequencing is managed by the 6001 module, a custom carrier needs only to provide a single 12V supply to the module, greatly simplifying the carrier design.

Memory Resources

The 6001 architecture supports up to a 10 GByte bank of DDR4 SDRAM memory accessible from the Programmable Logic. User-installed IP, which, along with the Pentek supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Up to an 8 GByte bank of DDR4 SDRAM is available to the Processing System as program memory and storage.



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PCI Express Interface

In many applications, the 6001 will be used with a PCIe interface provided by the carrier. The Pentek Navigator FDK library includes multiple DMA controllers for efficient transfers to and from the module.

Carrier Design Package

Pentek offers the Model 4801 Carrier Design Kit for users interested in designing their own carrier for the 6001 QuartzXM. The kit uses the Pentek Model 5950 3U OpenVPX carrier as a reference design. The kit includes:

- Pin definitions and electrical specifications of all signals on the module
- 3D models of the module
- Thermal profiles of the module and components
- Carrier reference design schematics
- PCB stack-up recommendations
- PCB design guidelines and routing rules
- Operating system and bootstrap guidelines
- Additional electrical and mechanical engineering guidance

Model 6001 QuartzXM customers must purchase the Model 5950 3U VPX carrier board, which includes the QuartzXM within an open-standard form factor. This allows the user to start IP development and proof of concept designs immediately on a known, tested platform while they develop their own carrier for later deployment. To further speed development tasks, Pentek offers a single-slot 3U VPX development chassis with the Model 5950 installed, along with a rear transition module (RTM) and all needed cables.

Optimized IP

Xilinx has created an integrated processing solution in the RFSoC that is unprecedented. The key to unlocking the potential of the RFSoC is efficient operation using optimized IP and application software. Pentek helps streamline the process from development to deployed application by providing a full suite of built-in functions. These address the data flow and basic processing needed for some of the most common applications. Please refer to the Model 5950 datasheet for descriptions of these built-in IP functions. For each example the board's included IP is all that is needed to demonstrate the application and may satisfy the full set of requirements for any particular application. These applications can also be the starting point for adding additional IP from the Pentek Navigator IP library or for adding custom IP.

Specifications

Field Programmable Gate Array
Xilinx Zynq UltraScale+ RFSoC XCZU27DR-1
Option -002: XCZU27DR-2, -2 speed grade

RFSoC RF Signal Chain

Analog Inputs:
Quantity: 8
Connector: Board-to-board, multi-channel differential
Input Type: Differential
Full Scale Input: 1Vp-p into 100 ohm on-die termination
3 dB Passband: 4 GHz

A/D Converters:
Quantity: 8
Sampling Rate: 4.0 GHz
Resolution: 12 bits

Digital Downconverters:
Quantity: 1 per A/D
Decimation Range: 1x, 2x, 4x and 8x
LO Tuning Freq. Resolution: 48 bits, 0 to f_s
Filter: 80% pass band, 89 dB stop-band attenuation

Analog Outputs:
Quantity: 8
Connector: Board-to-board, multi-channel differential
Input Type: Differential
Full Scale Output: 32 mA
3 dB Passband: 4 GHz

D/A Converters:
Quantity: 8
Sampling Rate: 6.4 GHz
Resolution: 14 bits

Digital Upconverters:
Quantity: 1 per D/A
Interpolation Range: 1x, 2x, 4x and 8x
LO Tuning Freq. Resolution: 48 bits
Filter: 80% pass band, 89 dB stop-band attenuation

Sample Clock: Received through board-to-board, multi-channel connector
Quantity: 4 A/D clocks, 2 D/A clocks

SysRef: Received through board-to-board, multi-channel connector

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RFSoC RF Processing System
- **ARM Cortex-A53:**
  - **Quantity:** 4
  - **Speed:** 1.5 GHz
- **ARM Cortex-R5:**
  - **Quantity:** 2
  - **Speed:** 600 MHz

QuartzXM Digital Connector (Programmable Logic)
- **Parallel:** 32 single ended or 16 pairs of LVDS connections
- **GTY:** 16 full duplex lanes @ 28 Gb/sec Processing
- **GPIO:** 8 single ended

QuartzXM Digital Connector (Processing System)
- **GTR:** 4 full duplex lanes
- **I2C:** Quantity 2
- **SPI:** Quantity 1
- **UART** Quantity 1
- **SD Card Interface:** Quantity 1
- **GPIO:** 8 single ended

Memory
- **Processing System:**
  - **Type:** DDR4 SDRAM
  - **Size: (standard)** 4 GBytes;
    - **Option 150:** 8 GBytes
  - **Speed:** 1200 MHz (2400 MHz DDR)
- **Programmable Logic:**
  - **Type:** DDR4 SDRAM
  - **Size: (standard)** 5 GBytes;
    - **Option 150:** 10 GBytes
  - **Speed:** 1200 MHz (2400 MHz DDR)

Environmental
- **Standard: L1**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -703: L3**
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

Size: 2.5 in. x 4 in. (63.5 mm x 101.6 mm)

Ordering Information

Model	Description
6001	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - QuartzXM

Options:

-002	-2 FPGA speed grade, -1 standard
-150	8 GBytes processor system memory, 10 GBytes programmable logic memory
-703	Environmental Level L3

Model	Description
4801	QuartzXM Carrier Design Kit

Contact Pentek for additional information about extended environmental levels

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