PCM BIT SYNCHRONIZER

BSM601

Features

- Bit Rates
  - 40 bps to 20 Mbps
- Performance within 1 dB of theory
- Four Loop bandwidth settings
- Traking up to 15%
- Accepts NRZ-L/M/S, RNRZ, BiØ-L/M/S, DM-M/S; MDM*
- 4 Input Sources
- Status Indicators for Sync and Input Signal Present
- Randomizer / Derandomizer lengths 2^N - 1:

  N = 9, 11, 15, 17, 20, 23
- Viterbi Decoder
- Frame Pattern Detector
- Fully Controlled from the VME Bus
- 6 U cPCI Form-factor

General Description

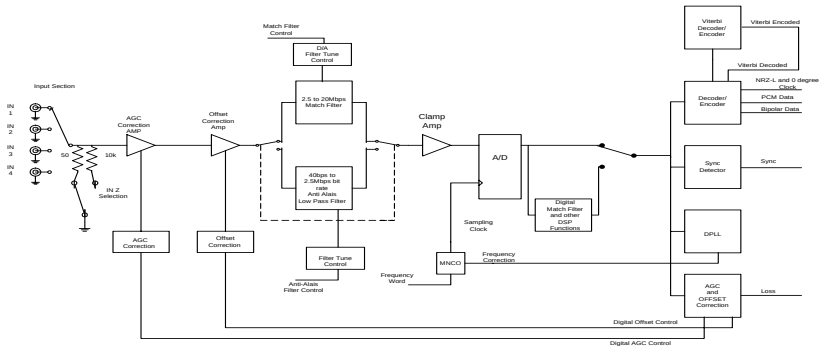
The GDP Model BSM601 PCM Bit Synchronizer is a state-of-the-art high-performance device that is designed to extract usable digital data from a noise contaminated signal environment. The optimized digital design of this unit affords the highest performance characteristics currently available.

The BSM601 is capable of maintaining synchronization with the signal of interest to Eb/No of -2 dB when the signal transition density is 50%. When searching for the signal, acquisition is attainable within 128 bits. The unit maintains synchronization for a period of at least 128 bit periods without a signal transition.

Encoded data streams are processed to expose the raw information. Randomized data is decoded to its native form by a pseudo-random decoder that handles lengths of 2 raised to the power 9, 11, 15, 17, 20 or 23. Both forward and reverse sequences are accommodated. Additionally, a Viterbi decoder (constraint length 7 rate 1/2) is included.

To add accuracy to the bit lock decision, the Viterbi decoder and / or the Frame Pattern Detector may be invoked.

To further assure synchronization to the intended data stream, the Frame Pattern Detector may be invoked. Up to a 32-bit long pattern is detected. Maintaining synchronization with this pattern at the programmed repetition rate produces a lock signal, which may be included in the bit-lock indication.



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SPECIFICATIONS

Signal Inputs

Inputs	Four (4)
Input Impedance	75 ohms (optional 50); High Z = 1k ohms
Levels	0.4 Vpp Min., +12 V and –12 V Max..(Others available)
DC Offsets	100% of the input peak-to-peak signal level.
AC Offset	No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Input Codes	NRZ-L/M/S, BIØ-L/M/S, DM-M/S,; MDM-M/S*
De-randomizer	RNRZ De-randomizer lengths of 9,11,15, 17, 20, 23 forward and reverse
Polarity	Input polarity normal / inverted.
Viterbi Decoder	Constraint length 7, rate ½, G1 =171 octal G2= 133 octal G1/G2 Swap and G2 Invert

Synchronization

Bit Rate Range	40 bps to 20 Mbps
Bit RateTuning Resolution	$X.XXXE^N$ ($1 \leq N \leq 7$)
Capture Range	Equal to LBW
Loop Bandwidths	Four (Damping constant 0.707)
Tracking	1% in Loop 1 (narrow) to 15% in loop 4 (wide)
Sync Threshold	SNR 0 dB for NRZ and BIØ codes, square-sided data.
Sync Maintenance	SNR –1 dB with transition density 50%, LBW1, NRZ-L
Sync Acquisition	128 bits or less
Sync Retention	128 bits without transitions, LBW1.
Bit Error Rate	≤ 1 dB to 20 Mbps
Frame Pattern Detector	Detection of up to 32 bits

Outputs

TTL - Clock & Data
RS422 - Clock & NRZ-L
Coded PCM Data
Bipolar Tape Output +/-1V - Coded PCM
LOCK STATUS - Bit Synchronization, Frame Pattern and Viterbi

R103102

Ordering Information

BSM602-00	Basic Unit (10 Mbps)	OPBSM62-20	Special PCM Codes (eg MDM)*
OPBSM62-02	Viterbi Decoder		
OPBSM62-03	Frame Pattern Detector		

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

The statements in this data sheet are not intended to create any warranty, expressed or implied. Equipment specifications are subject to change without notice.

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