DUAL PCM BIT SYNCHRONIZER on PCI

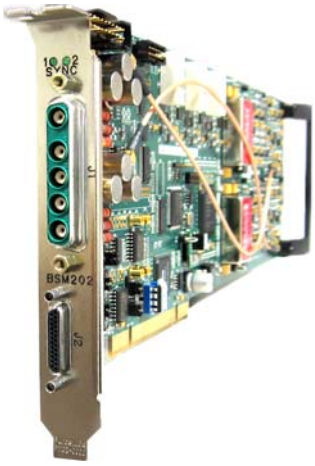
BSM202

Features

- Dual Channel (Single Channel Configurations available)
- Bit Rates
  - 5 bps to 20 Mbps (std)
  - 5 bps to 40 Mbps (opt)
- Performance within 1 dB of theory
- Loop bandwidth settings from 0.01% to 1.6%
- Tracking up to 15%
- Accepts NRZ-L/M/S, RNRZ, BiØ-L/M/S, DM-M/S MDM
- 2 Input Sources per Channel
- Status Indicators for Sync and Input Signal Present
- Randomizer / Derandomizer
- Scrabbler/Descrambler

  CCITT V.35/36
- Viterbi Decoder
- Frame Pattern Detector
- Signal Quality Status
  - Eb/No Measurement
  - Frame Sync Pattern Error Count (BER Status)
  - Viterbi Error Count
  - BERT/ PRN BER Measurement
- Advanced Lock Detection
- Auto Scan (Optional)
- Fully Controlled via RS-232 or RS-485 Remote Port or via from the PCI Bus
- PCI Form-factor (one slot)
- Additional Input & Output Options Available (Extended I/O)

General Description



The GDP Model BSM202 is a Dual Channel PCM Bit Synchronizer on a single PCI card (single channel configurations also available). The BSM202 is a state-of-the-art high-performance device that is designed to extract usable digital data from a noise contaminated signal environment. The optimized digital design of this unit affords the highest performance characteristics currently available.

The BSM202 is capable of maintaining synchronization with the signal of interest to Eb/No of -3 dB when the signal transition density is 50%. When searching for the signal, acquisition is attainable in less than 50 bits. The unit is very robust and can maintain synchronization for a period of at least 256 bit periods without a transition.

The standard IRIG randomizer/derandomizer for both forward and reverse sequences is provided. CCITT V.35 and V.36 scrambling/descrambling is also provided. A variety of Viterbi decoders are available including R1/2 K7 (Std), R3/4 K7 and R1/3 k7 (please inquire for other FEC options).

To assure synchronization to the intended data stream, the Frame Pattern Detector may be invoked. Up to a 64-bit long pattern is detected. Maintaining synchronization with this pattern at the programmed repetition rate and synchronization strategy produces a lock signal. An Automatic Polarity Correction (APC) mode is also provided for inverted data.

The BSM202 includes several unique features to determine the quality of the data. The first is an Eb/No (Signal Quality) measurement. From this measurement the error rate of the data can be determined. The BSM202 also measured errors in the frame synchronizer pattern as well as errors in the viterbi stream when these modes are enabled. A bit-error-rate (BERT) function is also provided. This allows link test in a short loop-back to verify proper operation of the module, or long loop-back to measure performance of the link. An advances lock detector ensures a solid lock indication for the module.

The Auto Scan feature is available to scan the input for up to 8 combinations of bit rates, input codes and frame patterns (per Bit Sync). When one of the signals is present the Bit Sync automatically locks onto it and recovers the data and clock.

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BSM202

SPECIFICATIONS

Inputs, each Bit Sync

Analog Inputs	Up to 2 Inputs per Bit Sync- 50 ohms (optional 75) or High Z (Transition Module Dependent)- Additional I/O Options Available
Digital Inputs	Differential RS-422 or TTL; (Optional)

Performance

Bit Rate Range	5bps to 20 Mbps (40 Mbps Optional)
Tuning Resolution	$X.XXXE^N$ ($1 \leq N \leq 7$)
Input Levels	0.1 Vpp Min., +/- 12 V Max.. (others available)
DC Offsets	100% of the input peak-to-peak signal level.
AC Offset	No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Loop Bandwidths	0.01% to 1.6%
Acquisition Range	2x LBW
Sync Acquisition Threshold	SNR 0 dB
Sync Maintenance	SNR –3dB
Sync Acquisition	< 50 bits
Sync Retention	256 bits without transitions
Bit Error Rate	1 dB to 40 Mbps

Features

Input/Output PCM Codes	NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S; MDM-M/S
Randomizer/Derandomizer	IRIG 106-96 forward and reverse
Descrambler	CCITT V.35/V.36
Viterbi Decoder	R 1/2, K 7 with G1/G2 Swap and G2 Invert, (others available)
Resequencer	QPSK/OQPSK/SOQPSK (Optional)
Frame Pattern Detector	Up to 64 bits with programmable strategy and APC
Auto Scan (Option)	Searches up to 8 Bit Rate, Code, Frame pattern combos per Bit Sync
Output Data Polarity	Input polarity normal / inverted.
Output Clock Phase	0, 90, 180, 270 degrees
BERT Function	Bit-Error-Rate PRN Generator/Error Detector

Outputs, each Bit Sync Channel

TTL Per Channel– Coded PCM and Clock (Programmable 0, 90, 180, 270 degrees)
2nd Output Per Channel: RS422 or TTL– Coded PCM and Clock (Programmable 0, 90, 180, 270 degrees)
Bipolar Tape Output +/-1V - Coded PCM
LOCK STATUS - Loss and Composite Lock (Bit Sync, Frame Pattern and Viterbi)
Signal Quality Status: Eb/No, Deviation, Frame Sync Pattern Error Count, Viterbi Error Count and BERT / PRN BER Measurements on Front Panel Display and Remote Port
Setup/Control: RS-232(Std), RS-485 (Opt), PCI Bus Control (Opt)

71009

Ordering Information

BSM202-00	Basic Dual Channel Unit (20 Mbps)	OPBSM202-43	BERT Option
OPBSM202-01	Extended bit rate to 40 Mbps	OPBSM202-45	Auto Scan Option
OPBSM202-05	QPSK & OQPSK Support	OPBSM202-48	Additional I/O Option
OPBSM202-06	SOQPSK Support	OPBSM202-70	75 ohm option
OPBSM202-10	RS-485 Serial Remote Control	OPBSM202-DR/XP	XP Driver
OPBSM202-11	RS-232 Serial Remote Control	OPBSM202-VI/XP	Virtual Interface (Remote SW)

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

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