

# Critical Techniques for High Speed A/D Converters in Real-Time Systems

**Eighth Edition** 

A/D Markets and Technology Sampling and Filtering Techniques FPGA Technology Products Ruggedized Products Applications Links

by

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#### **Preface**

An A/D (Analog-to-Digital) converter, frequently abbreviated as ADC, accepts an analog voltage at the input and produces a digital representation of that voltage at the output that's called a "sample".

The two primary characteristics of A/Ds are the rate of conversion or sampling rate, expressed in samples per second, and the accuracy of each digital sample expressed as the number of binary bits or decimal digits per sample.

Sampling rates vary tremendously between applications. A digital medical thermometer may deliver samples to update the readout once every five seconds while a high-speed wideband radar may produce 2 billion samples per second.

The difference in sample rates between these two prominent examples is a staggering 10 orders of magnitude. There are thousands of A/D applications spread continuously throughout this range.

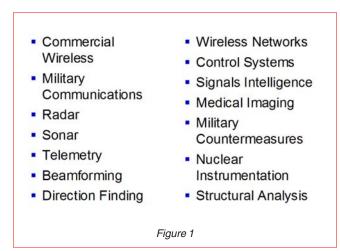
To help define the meaning of "high-speed A/D" used in this handbook, we will be focusing primarily on A/D converters with sampling rates higher than 100 MHz. We will review sampling techniques, FPGA technology and we will present the latest Pentek high-speed A/D products and applications based on them.

For more information on complementary subjects, the reader is referred to these other Pentek Handbooks: Software Defined Radio Handbook Putting FPGAs to Work in Software Radio Systems High-Speed Switched Serial Fabrics Improve System Design High-Speed, Real-Time Recording Systems



# A/D Markets and Technology

#### High Speed A/D Converter Markets



Markets for high-speed A/D converters are significant in size and many are growing rapidly. New markets emerge regularly based on A/D technology advances, lower costs, and the general trend of replacing older mechanical and analog systems with DSP (digital signal processing) systems.

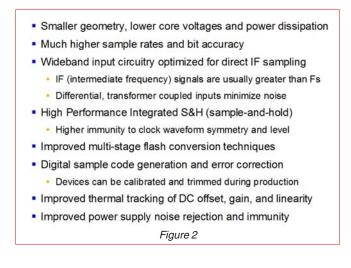
DSP offers significant advantages for handling signal complexity, communications security, improved accuracy and reliability, reduced size, weight and power.

Commercial users of high-speed A/Ds include wireless mobile communication systems, airline radar systems, air traffic control towers, ship communications, and wireless networks for home, office and public facilities.

Industrial uses include medical imaging systems and process control systems for manufacturing.

Government systems account for many of the highend applications such as phased-array military radar, communications countermeasure systems, global military radio networks, unmanned aerial vehicles and intelligence gathering systems.

#### New Monolithic A/D Technology



Because of the complexity of these market segments, wideband A/D converters have made significant advances in recent years.

This is due partly to silicon process improvements and also to many applications that require direct sampling of IF signals well above 100 MHz.

One of the most important advances is the sampleand-hold (or track-and-hold) circuitry at the front end.

Just as important, are new sample clock interfaces and drivers.

At these speeds, you need state-of-the-art flash and multistage flash conversion techniques.

New techniques in digital error code correction and thermal compensation circuitry help eliminate errors in bit accuracy, linearity and gain.

Lastly, these new devices are more immune to power supply and system noise.



# A/D Markets and Technology

#### Monolithic A/Ds for Fs Greater than 100 MHz and Bits Greater than Eight

Monolithic A/D Converters Manufacturer Part No. Sample Freq. Channels Bits Input BW									
Manufacturer	Part No.	sample Freq.	Cnanneis	Bits	Input BW				
Texas Instr.	ADC12D1800	3,600 MHz	1	12	1,750 MHz				
Linear Tech.	LTC2380-16	2,000 MHz	1	16	34 MHz				
Atmel	AT84AS008	2,000 MHz	1	10	3,000 MHz				
Texas Instr.	ADC12D1800	1,800 MHz	2	12	2,800 MHz				
Linear Tech.	LTC2379-18	1,600 MHz	1	18	34 MHz				
Maxim	MAX108	1,500 MHz	1	8	2,200 MHz				
Texas Instr.	ADC08D1000	1,000 MHz	2	8	1,700 MHz				
Atmel	AT84AD001B	1,000 MHz	2	8	1,500 MHz				
Maxim	MAX101A	500 MHz	1	8	1,200 MHz				
Atmel	AT84AD004	500 MHz	2	8	1,000 MHz				
Texas Instr.	AD\$5463	500 MHz	1	12	750 MHz				
Texas Instr.	AD\$5474	400 MHz	1	14	750 MHz				
Texas Instr.	AD\$5485	200 MHz	1	16	300 MHz				
Analog Dev.	AD9480	250 MHz	1	8	400 MHz				
Analog Dev.	AD9430	215 MHz	1	12	700 MHz				
Analog Dev.	AD9410	210 MHz	1	10	500 MHz				
Analog Dev.	AD9054	200 MHz	1	8	350 MHz				
Linear Tech.	LTC2255	125 MHz	1	14	300 MHz				
		Figure 3							

Shown in the table above are some representative examples of commercially available, monolithic A/D converters with sampling rates greater than 100 MHz and resolution of at least 8 bits.

All these devices are potential candidates for boardlevel products for embedded systems, such as those made by Pentek. We have listed the input bandwidth in this table to highlight the importance of these A/Ds in direct IF sampling applications, also known as undersampling.

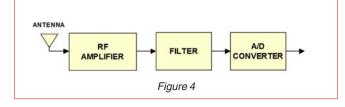
In the next section, we'll discuss in some detail the principles and rules of sampling.

Setting the Standard for Digital Signal Processing

## Sampling and Filtering Techniques

#### **Direct Baseband RF Signal Acquisition**

- Antenna signals are usually in the microvolt range
- RF amplifier boosts signal to full scale input voltage of the A/D - usually 0 to +10 dBm
- RF amplifier often includes a tuned bandpass filter centered on the signal of interest
- No analog frequency translation before the A/D
- Appropriate for HF signal frequencies (3 30 MHz)

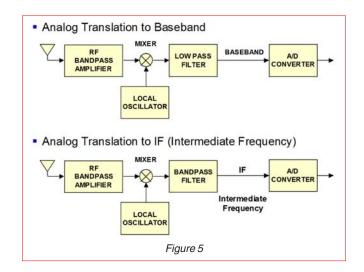


Most receiver systems start with a signal originating from an antenna that's often in the microvolt level, so it must first be amplified by an RF amplifier stage.

The amplifier is usually a tuned RF circuit which only passes the frequency band of interest, providing signal gain within that band and rejecting noise and unwanted signals in adjacent frequency bands.

If the RF input signal is at a low enough frequency, it can be digitized directly by an A/D converter, and no analog translation is necessary.

For example, you can usually perform direct baseband sampling on HF signals with no translation required, since the frequency content is below 30 MHz.



#### Analog RF Frequency Translation

In the case where the antenna signal frequency is too high to be digitized directly by the A/D converter, it has to be translated down using an analog mixer and local oscillator.

The top diagram shows a simplified representation of this analog translation to baseband with a low pass filter following the mixer.

The bottom diagram shows the translation to an intermediate frequency or IF — this is quite common. In this case, the filter is a bandpass filter centered at the IF frequency.

So far, we've discussed three types of front end circuitry:

1) Direct sampling with no translation

2) Analog translation to baseband

3) Analog translation to IF

But how do we design the filters in each case?

Let's go back to review some fundamental sampling theory.



# Sampling and Filtering Techniques

#### Filtering Helps Avoid Noise and Aliasing

- In all systems, the A/D input must be filtered for two important reasons:
  - Eliminate out of band noise
  - Eliminate aliasing
- Nyquist sampling theorem requires the input signal bandwidth must be less than one-half the sampling rate of the A/D converter
- Some systems (like an IF stage) provide inherent bandlimiting before the A/D
- Fundamental Sampling Modes
  - Baseband Wideband Sampling
  - Baseband Pre-select Sampling
  - Undersampling

Figure 6

Filters ahead of the A/D are needed primarily for two reasons: to eliminate out-of-band noise and to eliminate out-of-band signals that can cause aliasing.

Nyquist tells us that whenever you sample a signal with an A/D, the bandwidth of that signal must be less than half the sampling frequency of the A/D.

Filters help us guarantee that this rule is met. Sometimes the bandwidth is already limited by the signal source, like the output of an IF stage that takes advantage of the IF filter bandwidth. But each case has to be analyzed individually.

The design of the filter is also critically linked to the sampling mode. Here we've listed three fundamental sampling modes:

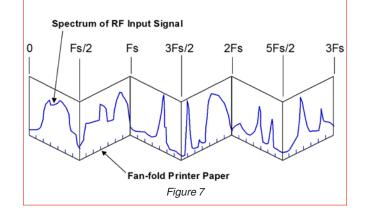
- 1) Baseband wideband sampling
- 2) Baseband preselect sampling

3) Undersampling, which is also sometimes called subsampling

To help you get a feel for the filter requirements of each mode, we present a convenient tool for analyzing the effects of sampling in the frequency domain.

#### Fan-fold Paper Model to Visualize Sampling

 Plot the spectrum of the input signal on transparent fan-fold printer paper scaled so the frequency axis is aligned with multiples of Fs on the backward folds



This simple technique has been very useful to our customers and our own applications engineers to help them understand what happens during sampling.

Imagine that we have a stack of the old fan-fold computer printer paper but with transparent sheets.

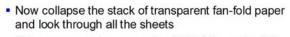
Now, we assign the frequency axis along the bottom edge of this paper, scaled so that multiples of the sampling frequency line up with the backward folds of the paper, as shown.

Using that frequency scale, we plot out the spectrum of the signal we want to sample with amplitude plotted on the vertical axis.

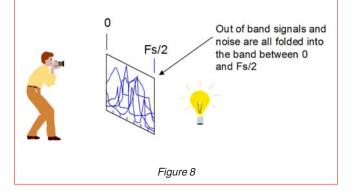
Setting the Standard for Digital Signal Processing

# Sampling and Filtering Techniques

### Fan-fold Paper Model to Visualize Sampling



- This represents how sampling "folds" the entire RF input spectrum into a single page from 0 to Fs/2
- · Once aliasing occurs, there is no way to undo it



Now, let's collapse the stack of transparent paper flat together and hold the stack up to a light so we can see through all the sheets.

We are now looking at the frequency plot of the sampled signal at the output of the A/D converter.

Notice that we've lost a lot of information because we can't tell which sheet a particular signal is on. And, unfortunately, after sampling that information is lost forever.

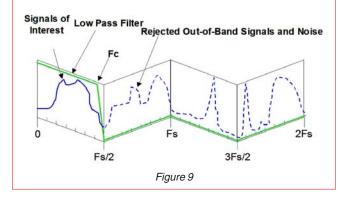
We've also contaminated any particular signal with signals from other sheets which have folded on top of it.

Not only that, we've also folded the noise from all the sheets so they pile up in the region between DC and the half sampling rate, potentially ruining the signal to noise ratio.

How do we avoid this mess in each of the three sampling modes?

#### **Baseband Sampling of Wideband Signals**

- For baseband signals over a wide frequency range, use a low pass filter with cutoff frequency, Fc, less than Fs/2, where Fs is the A/D sample rate
- After sampling, only the baseband signal is captured, eliminating folding of aliased signals and noise



For the baseband wideband sampling mode, where we want to look at everything from DC up to a frequency below the half sampling rate, we can install a low pass filter with a cutoff frequency, Fc, located below Fs/2.

The frequency response of the filter is shown in green.

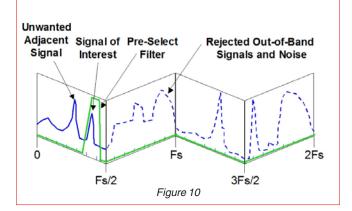
Now, all of the out-of-band signals and noise on the pages above Fs/2 are eliminated so that when the folding occurs, it doesn't corrupt the baseband signal.

Setting the Standard for Digital Signal Processing

## Sampling and Filtering Techniques

#### **Baseband Sampling of Preselect Signals**

- For narrowband signals at baseband, using a preselect bandpass filter can optimize the dynamic range of the A/D converter by rejecting strong adjacent signals and out-of-band signals and noise
- Pre-select filter is a bandpass filter whose passband is centered on the signal of interest



For the baseband **preselect** sampling mode, we need to use a bandpass filter with the frequency response shown in green.

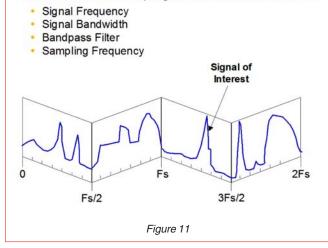
We get the same benefits as the previous case for out-of-band signals and noise above Fs/2, but more importantly, we can keep large adjacent signals like the one shown, from getting to the A/D converter.

The reason for this is that if the large unwanted signal gets through to the A/D converter, it uses up its dynamic range.

For applications where there are known, strong unwanted signals, this technique can be extremely useful in improving the signal-to-noise ratio of the smaller signal of interest.

#### **Principles of Undersampling**

- For narrowband signals above Fs/2, undersampling can be used to intentionally "alias" the input signal
- Very useful for IF outputs of UHF/VHF receivers
- Successful undersampling needs careful selection of:



The third sampling mode, called undersampling or subsampling, is ideal for many systems that use an analog RF translator front end. These receivers usually deliver IF outputs, often at 21.4 or 70 MHz, with bandwidths ranging from a few kilohertz to tens of MHz—depending on the receiver.

If we wanted to perform baseband sampling on a 70 MHz signal, we would have to choose a sampling rate of well over 140 MHz. This may require an A/D that adds significant cost and power to the system.

However, because the IF signal is inherently bandlimited, we can take advantage of the folding caused by sampling and use a lower frequency A/D.

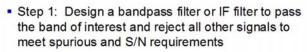
This is a little tricky since you have to carefully choose the sampling frequency and filtering according to the signal frequency and bandwidth.

Let's see how.

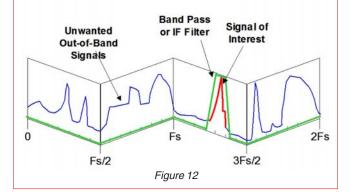


# Sampling and Filtering Techniques

#### Principles of Undersampling Design: Step 1



- Tradeoffs
  - Sharper filter adds complexity, expense, calibration, space, etc.
  - Sharper filter allows lower A/D sample rate



The fan-fold paper really comes in handy here.

First, design a bandpass filter that rejects unwanted signals and noise.

This is often fully satisfied by the standard IF filter in the RF translator, but you do have to check this.

Sharper filters add cost and maintenance but they do let you get away with a lower sampling rate as we'll see in the next figure.

Second (top of next column), choose a sampling frequency so that the passband of the filter, along with its skirts, falls entirely on a single page of fan fold paper.

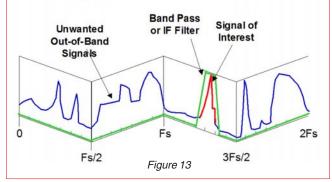
There are many possible solutions to each case, so you have to pick the one that works best. You may have to go back and forth a few times to readjust the filter and sampling rate to get the best scheme.

#### Principles of Undersampling Design: Step 2

 Step 2: Choose a sampling frequency so that the filter pass band and skirts fall entirely within one page of the fan-fold paper

#### Tradeoffs

- Higher sampling rate allows broader bandwidth & simpler filter
- A/D's with lower sampling rates are more accurate & less expensive



Here are some tradeoffs to consider:

With a higher sampling rate, the pages are wider and the filter becomes less complex. Also, there is a lower noise density folded into the 0 to Fs/2 band after sampling.

At higher sampling rates, however, the A/D is more expensive and the number of bits of accuracy drops off.

You also need to be sure that the A/D has a good wideband input stage to handle the IF signal with minimum distortion.

Equally important is the aperture uncertainty or phase jitter of the sample-and-hold amplifier, which is usually part of the A/D.

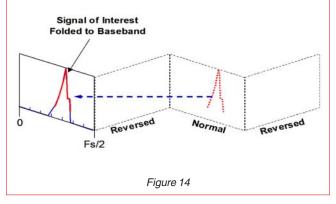
To make this job easier, many A/D converters are now specifically characterized to operate in undersampling applications.



# Sampling and Filtering Techniques

#### Undersampling Performs Frequency Translation

- Signal of interest folds into the 0 to Fs/2 region
- Undersampling performs an automatic frequency translation
- Translated image may be reversed in frequency depending on which side of the "fold" the input falls



The effect of undersampling, as you probably expected by now, is that the IF signal is folded down to the first page. This is really an automatic frequency translation, performed for free by the sampling process.

For the signals on every odd numbered sheet, the effect is a frequency translation by a multiple of Fs. For the signals on even numbered sheets, there is a reversal of the frequency axis on that sheet, followed by a translation by an odd multiple of Fs/2. Again, this is much easier to follow by visualizing the fan-fold model.

This undersampling technique is extremely popular in software radio systems which almost always follow the A/D converter with a DDC (digital downconverter).

Regardless of where the undersampling folding process translated the signal of interest, the DDC can translate it down to 0 Hz as a complex baseband signal. Once the complex signal is at baseband, the reversal of the frequency axis is easily undone by simply changing the sign of the Q component.

#### Guidelines for Sampling and Undersampling

- Use the fan fold paper to validate your sampling plan for the characteristics of your input signal
- Carefully evaluate A/D specifications for operation in the undersampling mode
- Ensure low-noise, wideband circuitry in the front end ahead of the A/D
- Transforming coupling often is superior to an amplifier for IF or RF input signals
- Eliminate as many out-of-band signals and noise as possible, since they will fold
- Ensure the the sample clock is clean with low phase noise and jitter

Figure 15

There are usually several different sample clock frequencies that will work for undersampling. While the fan-fold paper model can show all of the correct frequency plans, the best choice will usually be determined by several other important practical considerations shown above.

Some A/D converters are specifically characterized for undersampling applications, while others are designed only for baseband sampling. Make sure to verify the specifications.

Noise and distortion of the input signal must be minimized so these components don't fold into the sampled signal. Special care must be taken to preserve the purity of the sample clock signal.

Undersampling can be an extremely valuable tool for software radio applications, since it can eliminate at least one additional stage of analog frequency translation and simplify system design.

Undersampling allows you to use an A/D converter with a lower sampling rate, which usually means more bits of resolution and better dynamic range. This lower sample rate also reduces the cost and complexity of the next stage of digital signal processing, recording, storage, or transmission.



#### FPGAs: The Essential Companion for High Speed A/Ds

- 500+ MHz DSP slices and memory structures
- Over 3500 dedicated on-chip hardware multipliers
- On-board GHz serial transceivers
- Partial reconfigurability maintains operation during changes
- Switched fabric interface engines
- Over 690,000 logic cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC microcontroller cores
- Memory densities approaching 85 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 28 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards

#### Figure 16

FPGAs, or Field Programmable Gate Arrays, are commonly coupled to high speed A/Ds for two key reasons:

- They can perform real-time digital signal processing faster than general purpose programmable processors
- They offer extremely high-speed interfaces to other system components including built-in interfaces to high-speed switched serial fabrics.

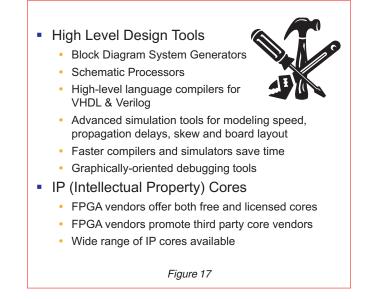
BGA and flip chip packages provide plenty of I/O pins to support these on-board gigabit serial transceivers and other user-configurable system interfaces.

Other important features are on-chip processor cores, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Dedicated hardware multipliers started appearing a few years ago and now you'll find literally thousands of them on chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking below 0.1 microns.





To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer many application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-tomarket crunch and to minimize risk.

11



#### FPGAs: Key Resources for DSP

Parallel Processing



- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Figure 18

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 3500 of them on a single FPGA.

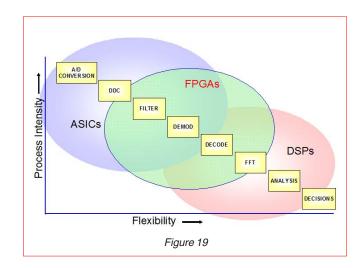
This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high- speed peripherals and buses.



# As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

# FPGAs Bridge the SDR Application Task Space



<b>FPGA Resource</b>	Comparison
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	Virtex-II Pro VP	<b>Virtex-4</b> FX, LX, SX	Virtex-5 LX, SX	<b>Virtex-6</b> LX, SX	Virtex-7 VX		
Logic Cells	53K–74K	55K-110K	52K-155K	128K–314K	326K–693K		
Slices*	23K–33K	24K–49K	8K–24K	20K-49K	51K–108K		
CLB Flip-Flops	46K–66K	48K–98K	32K–96K	160K-392K	408K-864K		
Block RAM (kb)	4,176–5,904	4,176–6,768	4,752–8,784	9,504–25,344	27,000–52,920		
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E	DSP48E		
DSP Slices	232–328	96–512	128–640	480–1,344	1,120–3,600		
Serial Gbit Transceivers	N/A	0–20	12–16	20–24	28–80		
PCI Express Support	N/A	N/A	N/A	Gen 2 x8	Gen 2 x8, Gen 3 x8		
User I/O	852–996	576–960	480–680	600–720	700–1,000		
*Virtex-II Pro and Virtex-4 Slices actually represent 2.25 Logic Cells; *Virtex-5, Virtex-6 and Virtex-7 Slices actually represent 6.4 Logic Cells							
Figure 20							

The above chart compares the available resources in the five Xilinx FPGA families that are used in most of

- the Pentek products. • Virtex-II Pro: VP
  - Virtex-4: FX, LX and SX
  - Virtex-5: LX and SX
  - Virtex-6: LX and SX
  - Virtex-7: VX

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethenet ports.

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

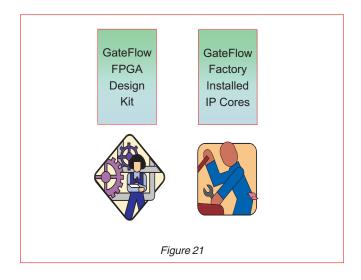
The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 500 MHz in V-4, to 550 MHz in V-5, to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.



#### Pentek GateFlow FPGA Design Resources



GateFlow<sup>®</sup> is Pentek's flagship collection of FPGA Design Resources. The GateFlow line is compatible with the Xilinx Virtex products and is available as two separate offerings:

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

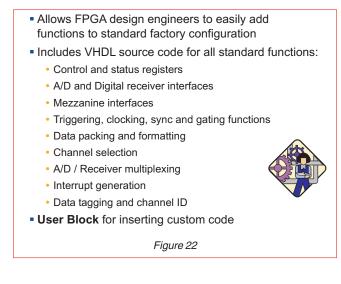
We also offer popular high-performance signal-processing algorithms with the GateFlow factory-installed IP Cores. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products

Installed Cores are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully supported with Pentek ReadyFlow<sup>®</sup> Board Support Packages.

Let's start with the GateFlow FPGA Design Kit.



#### GateFlow FPGA Design Kit



If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, and data tagging.

These are also fully supported with our ReadyFlow Board Support Package.



#### **î** 1 Front Panel Interfa User Application Sync Bus **Factory Installed** Timestamr **Base Function Application** A/D & D/A Control Data Packing & Formatting Meta Data Files Memory Linked-List A/D Control Linked-List D/A Control Memory Defined and P16 MGTs documented Registers LVDS interface signals Global Registers PCI Express Backend FLASH Interface V-6 or V-7 FPGA PCI Express Interface Figure 23

#### GateFlow FPGA Design Kit for Cobalt or Onyx Products

**FPGA** Technology

The **GateFlow** FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signalprocessing algorithms.

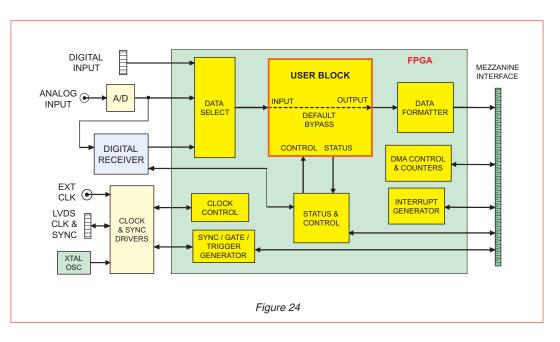
The Cobalt and Onyx architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware. Shown here is the FPGA block diagram of a typical Cobalt or Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



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#### GateFlow FPGA Design Kit for Other Pentek Products

**FPGA** Technology

The GateFlow FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

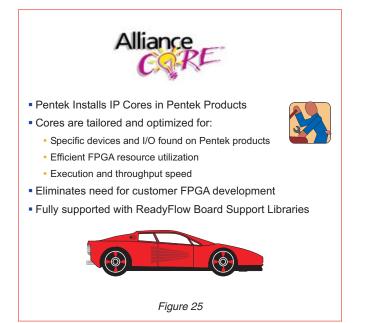
Shown above is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it. The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.





### **GateFlow Installed IP Cores**



Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

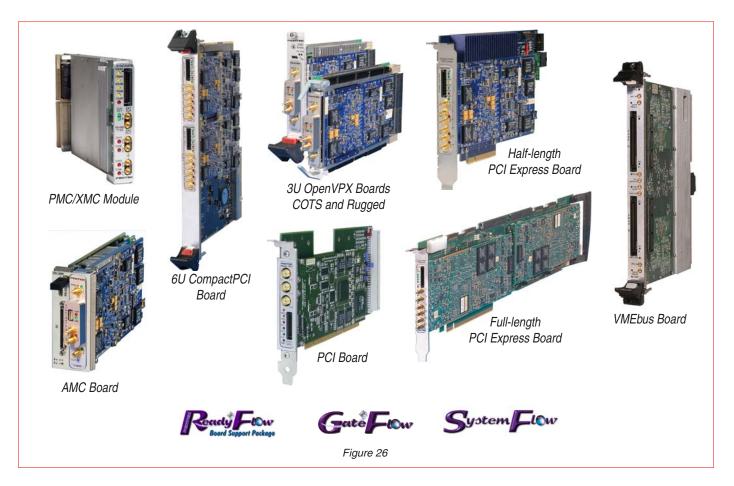
Pentek offers popular high-performance signal processing algorithms installed in Pentek products. These algorithms are designed expressly for Xilinx FPGAs and Pentek harware products. The cores take full advantage of the numerous hardware multipliers to achieve highlyparallel processing structures that can dramatically outperform programmable RISC and DSP processors.

Installed Cores are optimized for efficient FPGA resource utilization, execution and throughput speed. They are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully tested and supported with the Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.

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### PMC, XMC, CompactPCI, PCI, PCI Express, OpenVPX, AMC, and VMEbus Software Radio



The Pentek family of board-level analog I/O products is the most comprehensive in the industry. Most of these products are available in several formats to satisfy a wide range of requirements.

In addition to their commercial versions, many of these products are available in commercial, ruggedized and conduction-cooled versions.

All of the analog I/O products include input A/D converters. Some of these products are also software radio receivers in that they include DDCs. Others are software radio transceivers because they include DDCs as well as DUCs with output D/A converters. These come with independent input and output clocks.

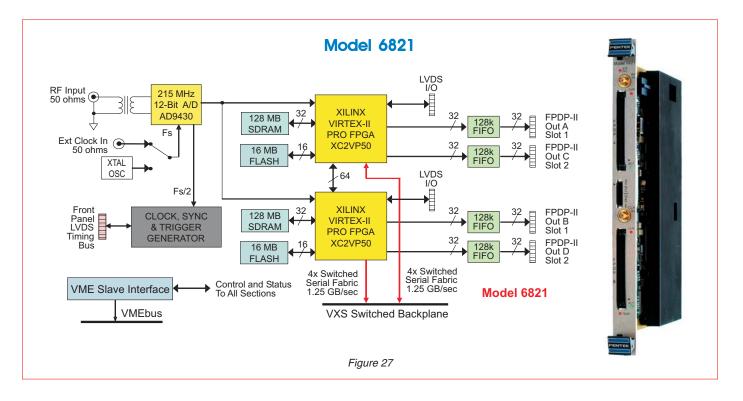
All Pentek analog I/O products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow<sup>®</sup> Board Support Package, the GateFlow<sup>®</sup> FPGA Design Kit and high-performance factoryinstalled IP cores that expand the features and range of many Pentek board-level products. In addition, Pentek recording systems are supported with SystemFlow<sup>®</sup> recording software that features a Windows<sup>®</sup> graphical user interface.

In addition to product overviews presented in the pages that follow, a complete listing of these products with active links to their datasheets on Pentek's website is included at the end of this handbook.



#### 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS



The Model 6821 is a 6U single slot board with the AD9430 12-bit 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers. Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

Optional 4X switched serial fabric ports, compliant with the VITA 41 VXS backplane fabric standard, deliver data to VXS devices using two full-duplex 1.25 GB/sec data ports.

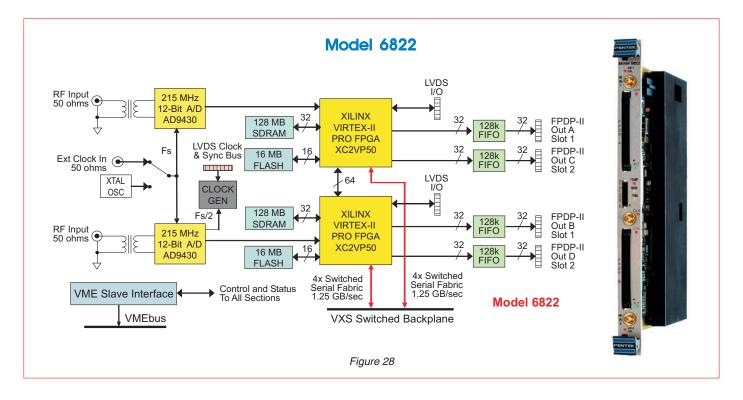
Since the switched fabric interface is implemented using the Rocket I/O gigabit serial transceivers in the FPGAs, the Model 6821 can support any of the switched fabric protocols including Serial RapidIO, PCI Express or the lightweight point-to-point link layer protocol, Aurora.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications.

This Model is also available in commercial as well as conduction-cooled versions.



#### Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS



The Model 6822 is a 6U single slot board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers. Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

Optional 4X switched serial fabric ports, compliant with the VITA 41 VXS backplane fabric standard, deliver data to VXS devices using two full-duplex 1.25 GB/sec data ports.

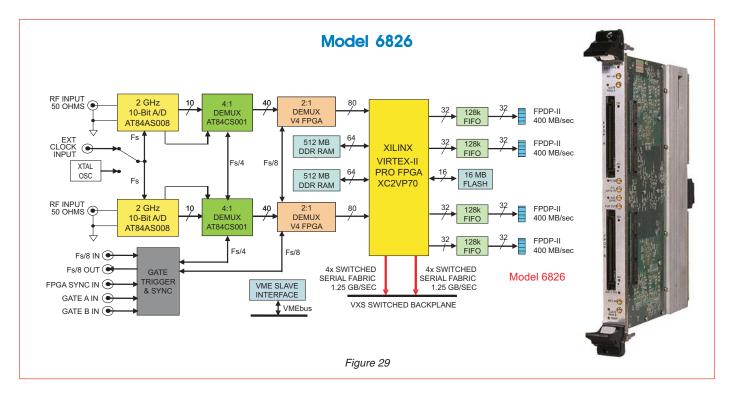
Since the switched fabric interface is implemented using the Rocket I/O gigabit serial transceivers in the FPGAs, the Model 6822 can support any of the switched fabric protocols including Serial RapidIO, PCI Express, or the lightweight point-to-point link layer protocol Aurora.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications.

This Model is also available in commercial as well as conduction-cooled versions.



#### Dual 2 GHz A/D with Xilinx Virtex-II Pro FPGA - VME/VXS



The Model 6826 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital

filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGA to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGA over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

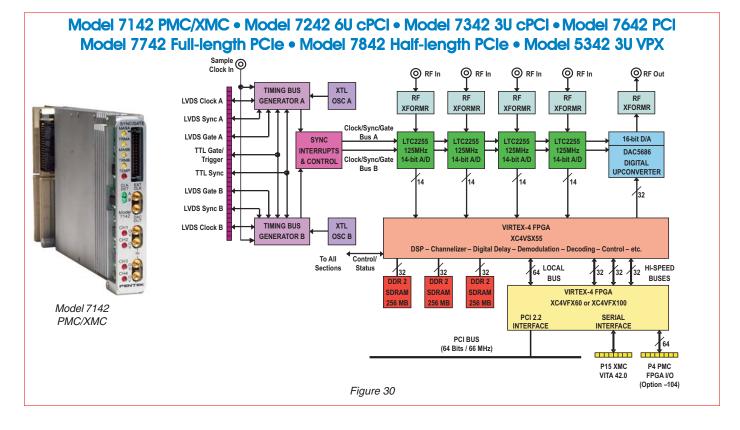
The 400 MB/sec FPDP ports run out of speed at an A/D sample rate of 1.6 GHz for one channel.

With VXS, however, the two 1.25 GB/sec ports can maintain continuous streaming data at up to 2.5 GB/sec, nicely handling the full 2 GHz A/D speed for one channel.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.



#### **Multichannel Transceivers**



The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA. A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

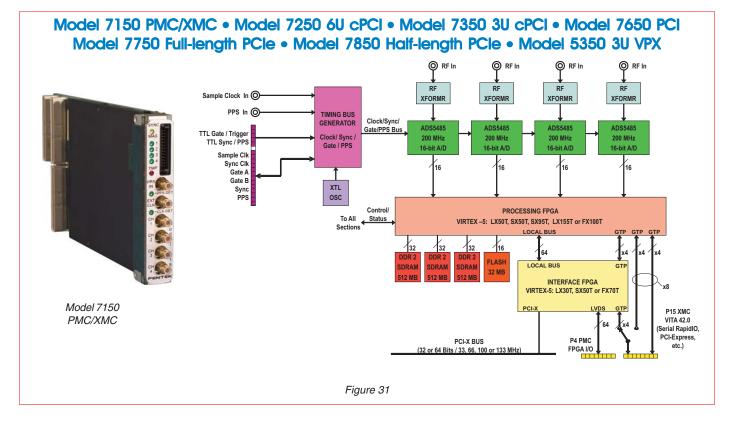
Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe fulllength board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), 3U VPX (Model 5342), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).



#### Quad 200 MHz 16-bit A/D with Virtex-5 FPGAs



Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources idealy matched to the requirements of high-performance systems. Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched fabric interfaces.

The Model 7150 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Three independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 9-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

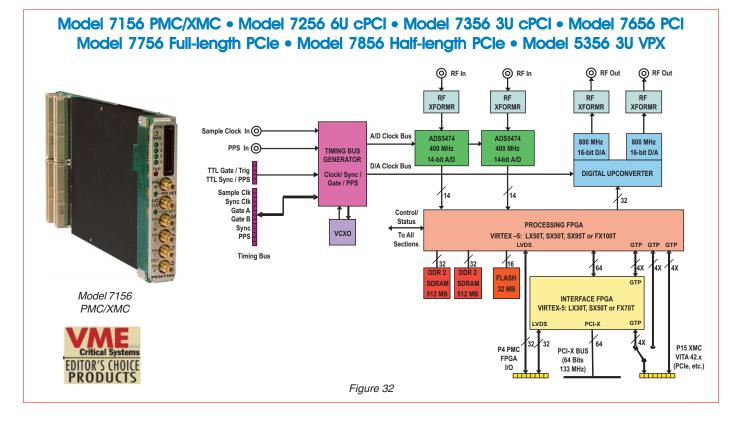
Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7150 are also available as a PCIe fulllength board (Models 7750 and 7750D dual density), PCIe half-length board (Model 7850), PCI board (Model 7650), 6U cPCI (Models 7250 and 7250D dual density), 3U cPCI (Model 7350), and 3U VPX (Model 5350).



#### Dual 400 MHz 14-bit A/D and 800 MHz D/A with Virtex-5 FPGAs



Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface. A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

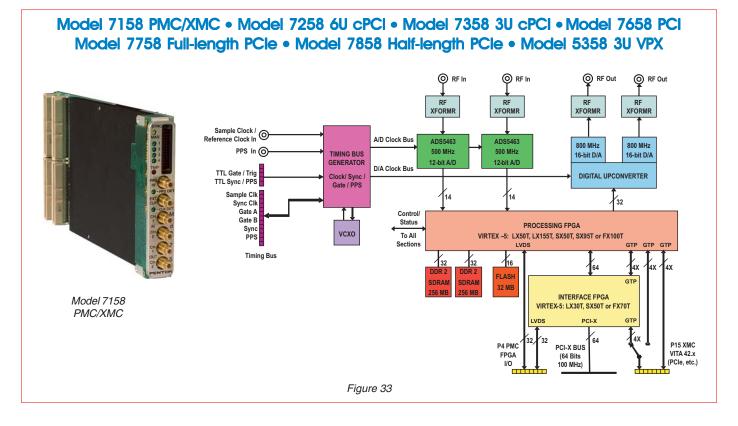
Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe fulllength board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), 3U cPCI (Model 7356), and 3U VPX (Model 5356). All these products have similar features.



#### Dual 500 MHz 12-bit A/D and 800 MHz D/A with Virtex-5 FPGAs



Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

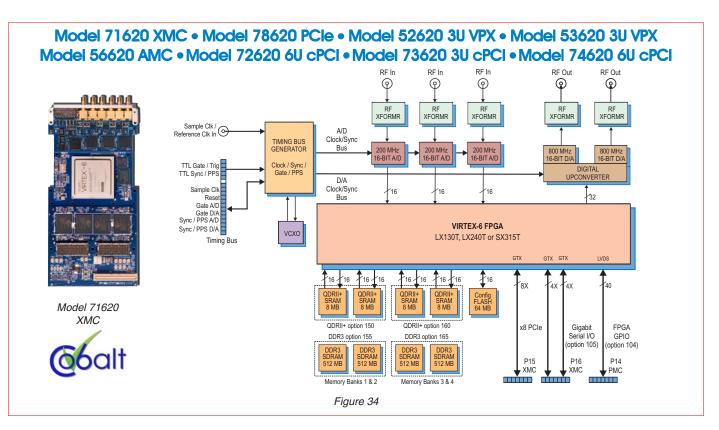
Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface. A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe fulllength board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), 3U cPCI (Model 7358), and 3U VPX (Model 5358). All these products have similar features.





#### 3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

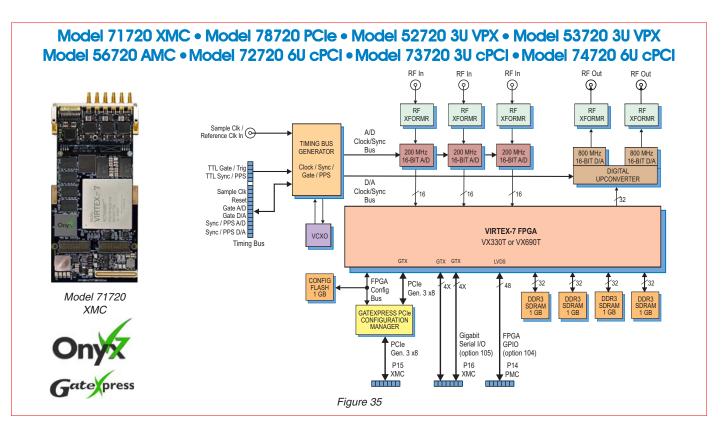
Model 71620 is a member of the Cobalt<sup>®</sup> family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for applicationspecific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factoryinstalled functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71620 are also available as a PCIe halflength board (Model 78620), 3U VPX (Models 52620 and 53620), AMC (Model 56620), 6U cPCI (Models 72620 and 74620 with dual density), and 3U cPCI (Model 73620).





#### 3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 71720 is a member of the Onyx<sup>®</sup> family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes generalpurpose and gigabit-serial connectors for applicationspecific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

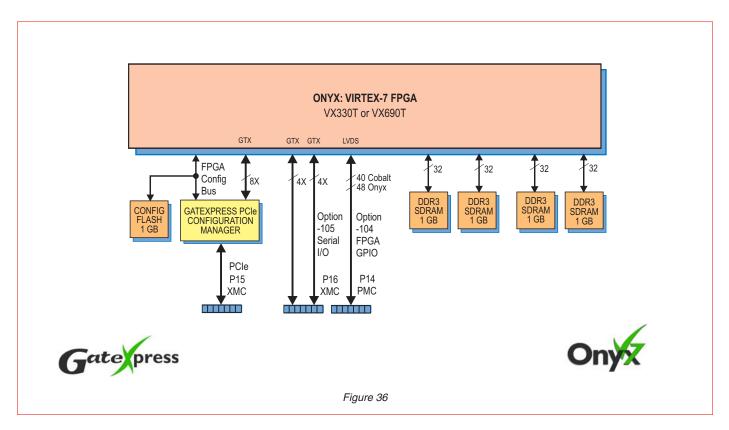
Multiple 71720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Versions of the 71720 are also available as a PCIe half-length board (Model 78720), 3U VPX (Models 52720 and 53720), AMC (Model 56720), 6U cPCI (Models 72720 and 74720 with dual density), and 3U cPCI (Model 73720).

GateXpress<sup>®</sup> is a sophisticated configuration manager for loading and reloading the Virtex-7 FPGA. More information is available in the next page.



#### GateXpress for FPGA-PCIe Configuration Management



The Onyx architecture includes GateXpress<sup>®</sup>, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

#### 1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA

Model 78630 PCIe • Model 71630 XMC • Model 52630 3U VPX • Model 53630 3U VPX Model 56630 AMC • Model 72630 6U cPCI • Model 73630 3U cPCI • Model 74630 6U cPCI RF Out RF In  $\odot$  $\odot$ RF XFORMR RF XFORMR Sample Clk / Reference Clk In PPS/Gate/Sync TIMING BUS A/D Clock/Sync Bus 1 GHz 12-BIT A/D GENERATOR Gate In Sync In 1 GHz Clock / Sync / Gate / PPS 6-BIT D// D/A Clock/Sync Bus A/D Sync Bus Gate In Sync In 12 D/A Sync Bus VIRTEX-6 FPGA LX130T, LX240T or SX3151 VCXO 16 16 716 116 ₹16 Model 78630 4X 4) x8 PCIe Optional Optional Memory Banks 3 & 4 DDR3 option 165 Memory Banks 1 & 2 DDR3 option 155 FPGA GPIO x8 PCle Serial I/O Dual 4X SRAM 8 MB 68-pin Serial Conn QDRII+ option 150 x8 PCI Express Figure 37

Model 78630 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application- specific I/O protocols.

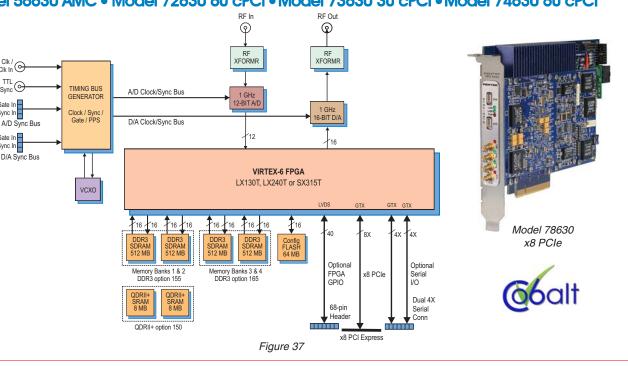
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factoryinstalled functions.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

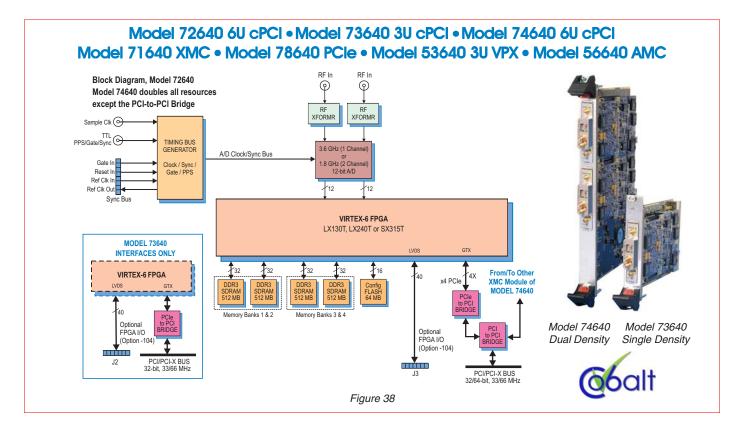
Versions of the 78630 are also available as an XMC module (Model 71630), 3U VPX (Models 52630 and 53630), AMC (Model 56630), 6U cPCI (Models 72630 and 74630 with dual density), and 3U cPCI (Model 73630).







#### 1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA



Models 72640, 73640 and 74640 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

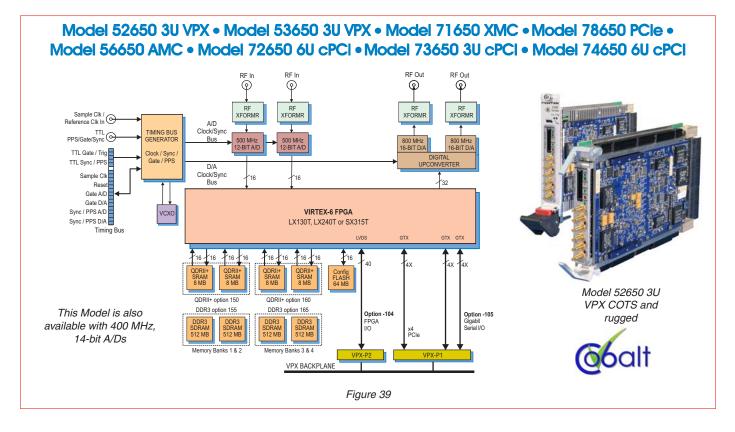
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 is a dual density 6U cPCI board. Also available is an XMC module (Model 71640), PCIe half-length board (Model 78640), 3U VPX (Models 52640 and 53640), and AMC (Model 56640).



#### 2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA



Model 52650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 52650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factoryinstalled functions.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 52650 are also available as a 3U VPX (Model 53650), XMC module (Model 71650), as a PCIe board (Model 78650), AMC (Model 56650), 6U cPCI (Models 72650 and 74650 dual density), and 3U cPCI (Model 73650).



#### Model 71660 XMC • Model 78660 PCIe • Model 52660 3U VPX • Model 53660 3U VPX Model 56660 AMC • Model 72660 6U cPCI • Model 73660 3U cPCI • Model 74660 6U cPCI RF In RF In RF In $\odot$ $\odot$ $\odot$ 0 AAAAAA RF XFORMR XFORMR XFORMR XFORMR Sample Clk / Reference Clk In O Gate / Trigger / Sync / PPS FIMING BUS A/D Clock/Sync Bus GENERATOR 200 MHz 16-BIT A/[ 200 MH2 6-BIT A/ 200 MHz 6-BIT A/D 200 MHz 16-BIT A/D TTL Gate / Trig TTL Sync / PPS Clock / Sync / Gate / PPS Sample Clk <sup>′</sup>16 <sup>^</sup>16 **´**16 16 Rese Gate A Gate E Sync / PPS A VIRTEX-6 FPGA Sync / PPS B vcxo LX130T, LX240T or SX315T Timing Bus GT 16 16 16 16 716 8X 43 4X Model 71660 XMC QDRII+ option 150 QDRII+ option 160 x8 PCle Gigabit Serial I/O FPGA GPIO DDR3 option 155 DDR3 option 165 option 104) option 105) DDR3 SDRAN 512 MB DDR3 SDRAM 512 MB P14 P15 P16 512 M 512 MF ХМС XMC PMC Memory Banks 1 & 2 Memory Banks 3 & 4 Figure 40

#### 4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

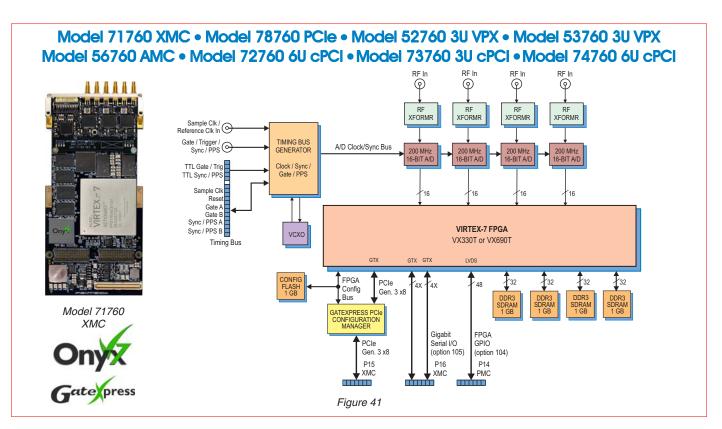
Model 71660 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71660 are also available as a PCIe halflength board (Model 78660), 3U VPX (Models 52660 and 53660), AMC (Model 56660), 6U cPCI (Models 72660 and 74660 with dual density), and 3U cPCI (Model 73660).





#### 4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA

Model 71760 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Onyx family is delivered with factoryinstalled applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factoryinstalled functions.

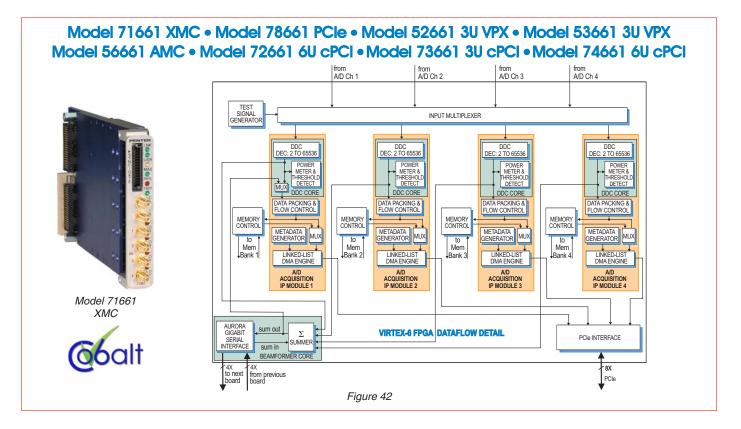
The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 71760 are also available as a PCIe halflength board (Model 78760), 3U VPX (Models 52760 and 53760), AMC (Model 56760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).

Please go to page 28 for information about GateXpress.



#### 4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA



Model 71661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

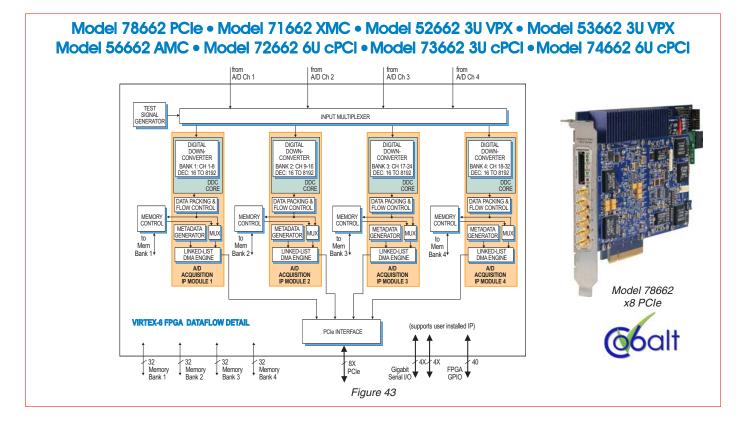
The 71661 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the 71661 are also available as a PCIe halflength board (Model 78661), 3U VPX (Models 52661 and 53661), AMC (Model 56661), 6U cPCI (Models 72661 and 74661 with dual density), and 3U cPCI (Model 73661).



#### 4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA



Model 78662 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192 programmable in steps

of eight. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

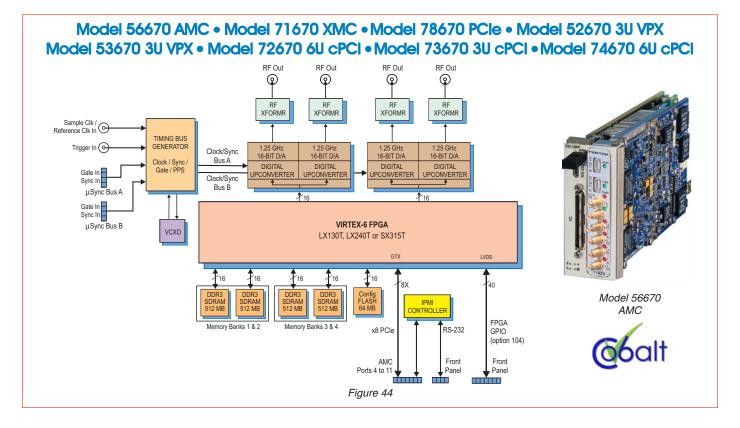
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8*f_s/N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of  $f_s/N$ . Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 78662 are also available as an XMC module (Model 71662), 3U VPX (Models 52662 & 53662), AMC (Model 56662), 6U cPCI (Models 72662 and 74662 with dual density), and 3U cPCI (Model 73662).



#### 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA



Model 56670 is a member of the Cobalt family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

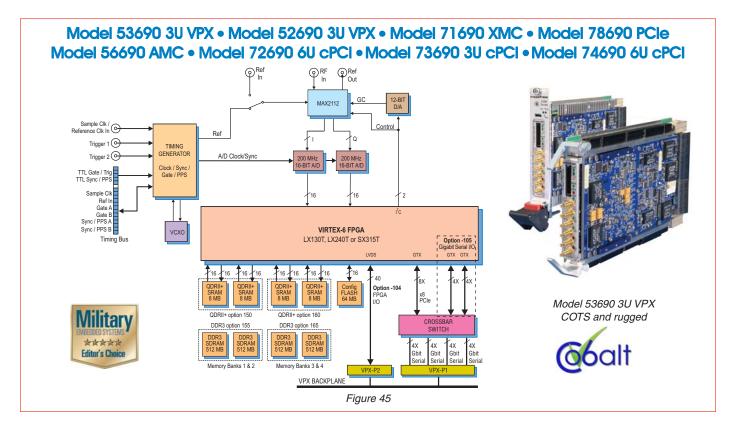
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

The Model 56670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Versions of the 56670 are available as an XMC (Model 71670), PCIe half-length board (Model 78670), 3U VPX (Models 52670 and 53670), 6U cPCI (Models 72670 and 74670 dual density), and 3U cPCI (Model 73670).



#### L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA



Model 53690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the

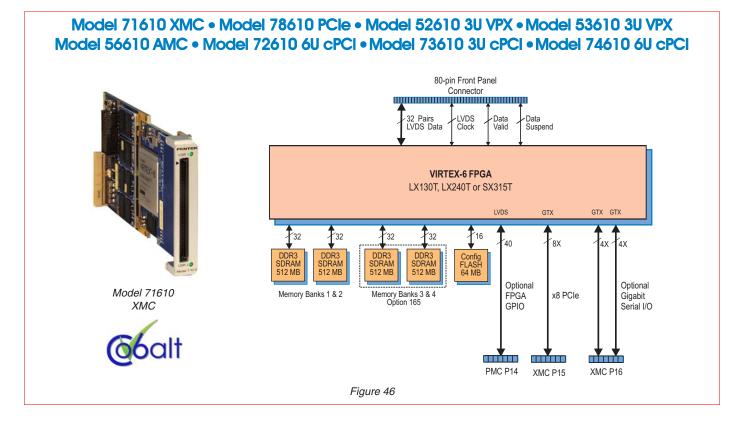
board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the 53690 are also available as a 3U VPX (Model 52690), an XMC (Model 71690), as a PCIe (Model 78690), AMC (Model 56690), 6U cPCI (Models 72690 and 74690 with dual density), and 3U cPCI (Model 73690).



### LVDS Digital I/O with Virtex-6 FPGA



Model 71610 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGAprocessing IP.

In addition to supporting PCI Express as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Versions of the 71610 are also available as a PCIe board (Model 78610), 3U VPX (Models 52610 and 53610), AMC (Model 56610), 6U cPCI (Models 72610 and 74610 with dual density), and 3U cPCI (Model 73610).



#### Model 71611 XMC • Model 78611 PCIe • Model 53611 3U VPX • Model 53611 3U VPX Model 56611 AMC • Model 72611 6U cPCI • Model 73611 3U cPCI • Model 74611 6U cPCI CH 2 CH 3 CH 4 RX TX RX TX FIBER OPTIC TRANSCEIVER FIBER OPTIC TRANSCEIVER FIBER OPTIC FIBER OPTIC TRANSCEIVER GTX GTX GTX GTX **VIRTEX-6 FPGA** LX240T, LX365T, SX315T or SX475T GTX פסעו 32 32 32 ₹16 32 40 8x Config FLASH 64 MB DRAM RAN Model 71611 512 ME 512 ME 12 MB 512 ME XMC FPGA Memory Banks 1 & 2 Memory Banks 3 & 4 x8 PCle GPIO DDR3 option 155 DDR3 option 165 (option -104) P15 P14 PMC XMC Figure 47

#### Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA

Model 71611 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, gigabit serial interface, it is ideal for interfacing to serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general purpose connector for application-specific I/O.

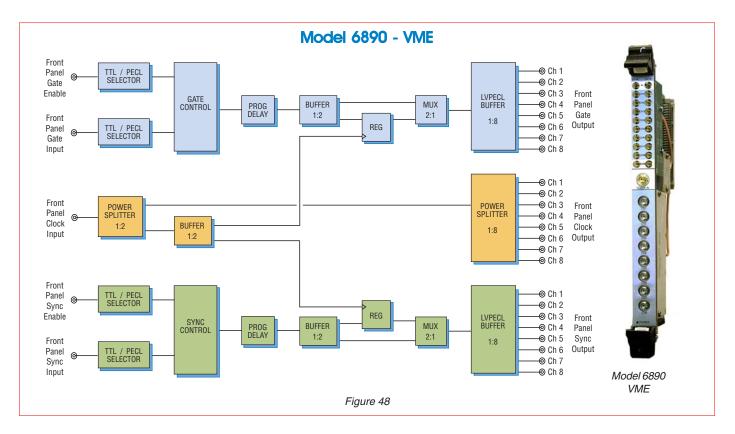
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factoryinstalled functions and enable the 71611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop.

Versions of the 71611 are also available as a PCIe board (Model 78611), 3U VPX (Models 52611 and 53611), AMC (Model 56611), 6U cPCI (Models 72611 and 74611 with dual density), and 3U cPCI (Model 73611).





#### 2.2 GHz Clock, Sync and Gate Distribution Board

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

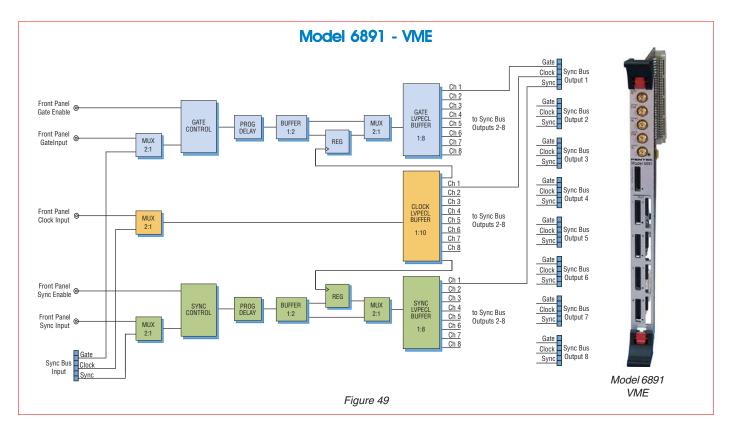
A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/ trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.



## System Synchronizer and Distribution Board



Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

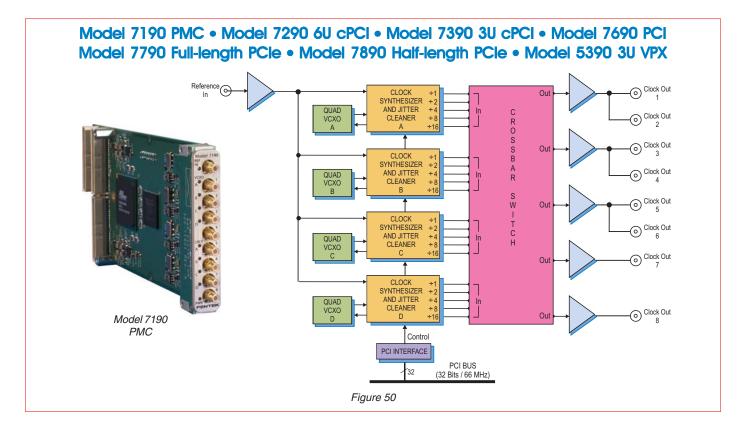
Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.



#### **Multifrequency Clock Synthesizer**



Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs and can be phase-locked to an external reference signal.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 MHz and 700 MHz.

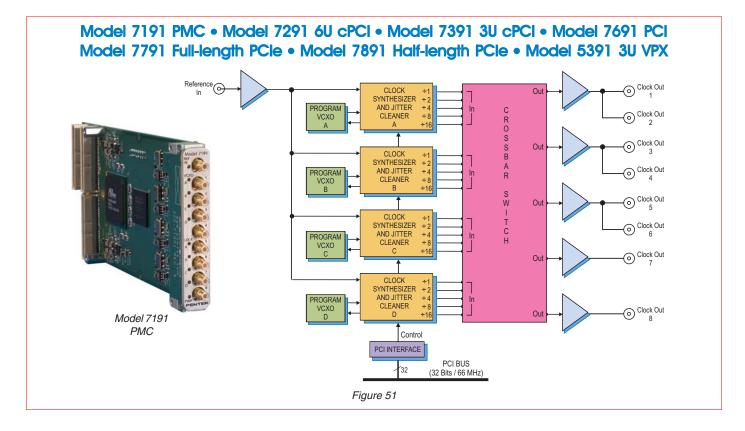
The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers. The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7190 are also available as a PCIe fulllength board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), 3U VPX board (Model 5390), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).



#### Programmable Multifrequency Clock Synthesizer



Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers. The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7191 are also available as a PCIe fulllength board (Models 7791 and 7791D dual density), PCIe half-length board (Model 7891), 3U VPX board (Model 5391), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).



#### Model 7192 PMC/XMC • Model 7892 Half-length PCIe • Model 5292 3U VPX Model 7292 6U cPCI • Model 7392 3U cPCI • Model 7492 6U cPCI PROGRAMMABI F VCXO Sample Clk Reference Clk In MU> Clock / Calibration Out $\odot$ PLL ✐ & DIVIDER uSvnc 1 . eference Clk In \* TWSI Control In TWS Gate / Trigger Out CONTROL Sync Out Reference Clk Out μSync 2 Gate / Trigger Out Svnc Out Reference Clk Out BUFFER Svnc 3 Gate / Trigger In PROGRAM Gate / Trigger Out $\odot$ Model 7192 Sync Out Reference Clk Out Sync In PMC/XMC uSvnc 4 Gate / Trigger Out Sync Out eference Clk Out \* For 71640 A/D calibration Figure 52

#### High-Speed Synchronizer and Distribution Board

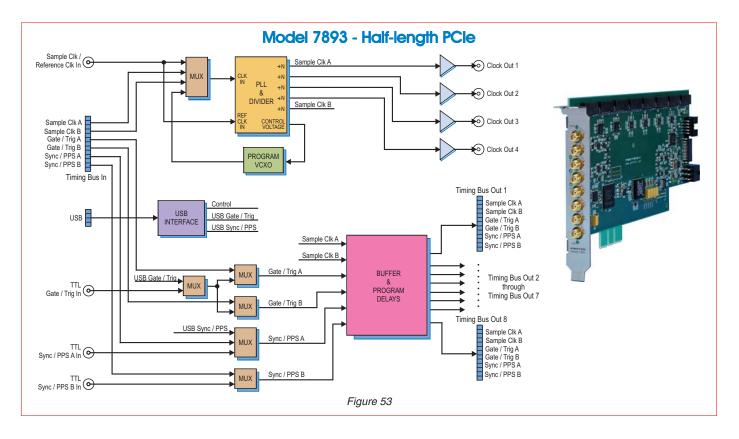
The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system. The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Fourchannel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Versions of the 7192 are also available as a PCIe halflength board (Model 7892), 3U VPX (Model 5292), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).





#### System Synchronizer and Distribution Board

Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

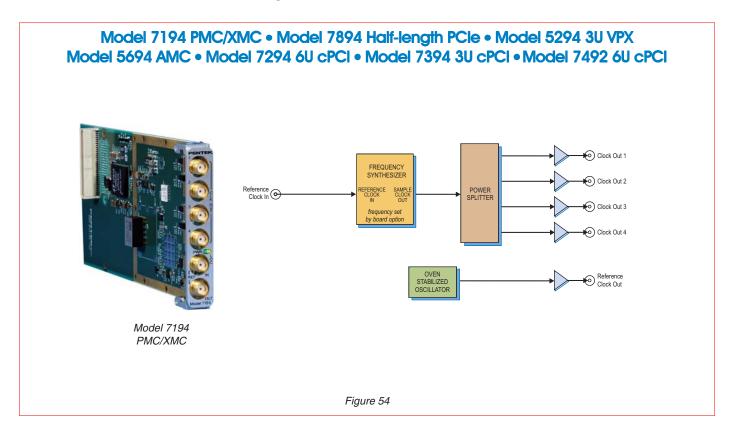
The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/ Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source. The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 fourchannel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.



### **High-Speed Clock Generator**



Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

The Model 7194 uses a high-precision, fixedfrequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

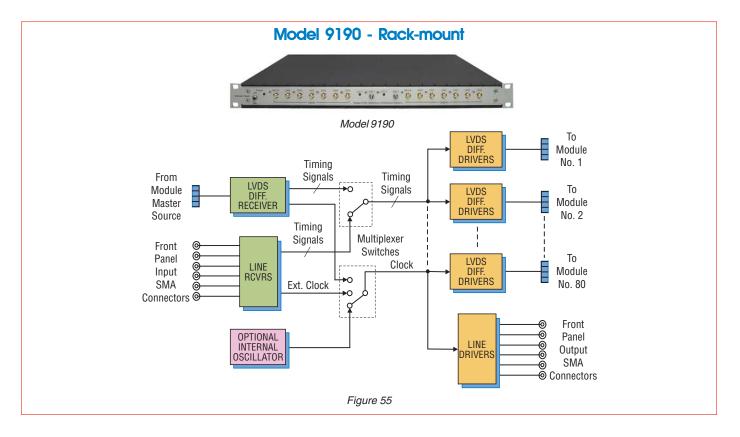
In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power. The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Versions of the 7194 are also available as a PCIe halflength board (Model 7894), 3U VPX (Model 5294), AMC (Model 5694), 6U cPCI (Models 7294 and 7494 dual density), and 3U cPCI (Model 7394).



#### Clock and Sync Generator for I/O Modules



Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

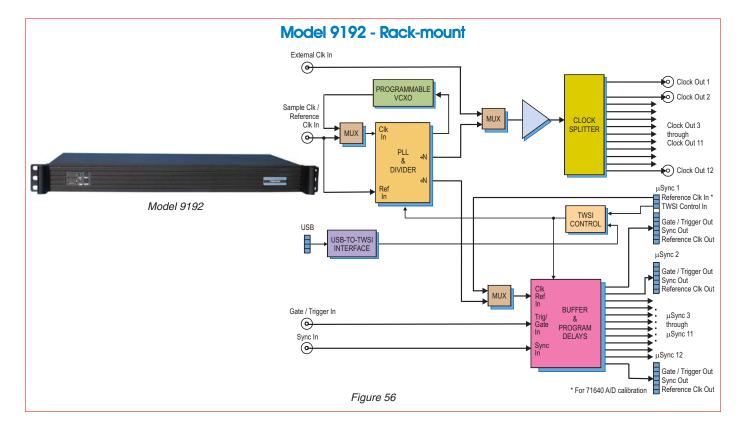
Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190. Buffered versions of the clock and five timing signals are available as outputs on the 9190's front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.



## High-Speed System Synchronizer Unit



Model 9192 Rack-mount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system. The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

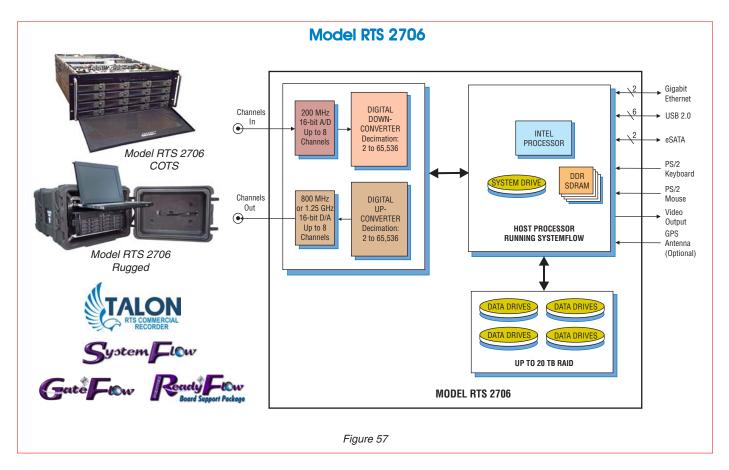
The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support highspeed models in the Onyx family as they become available.



## Eight-Channel RF/IF, 200 MS/sec Rackmount Recorder



The Talon® RTS 2706 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2706 uses 16-bit, 200 MHz A/D converters and provides sustained recording rates up to 2.0 GB/sec in four-channel configuration.

The RTS 2706 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

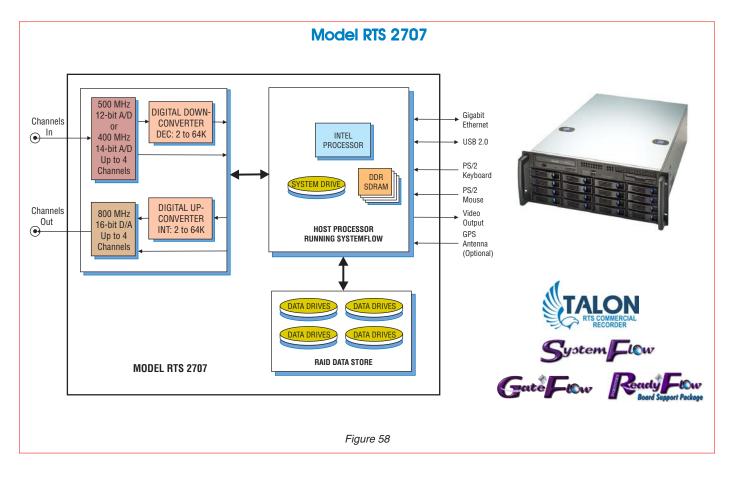
A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fullyprogrammable system capable of recording and reproducing a wide range of signals. Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Built on a Windows® 7 Professional workstation with high performance Intel® Core<sup>TM</sup> i7 processor, the RTS 2706 allows the user to install post-processing and analysis tools to operate on the recorded data. The instrument records data to the native NTFS file system, providing immediate access to the data.

The RTS 2706 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.



## Four-Channel RF/IF, 500 MS/sec Rackmount Recorder



The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides sustained recording rates up to 1.6 GB/sec in two-channel configuration.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fullyprogrammable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

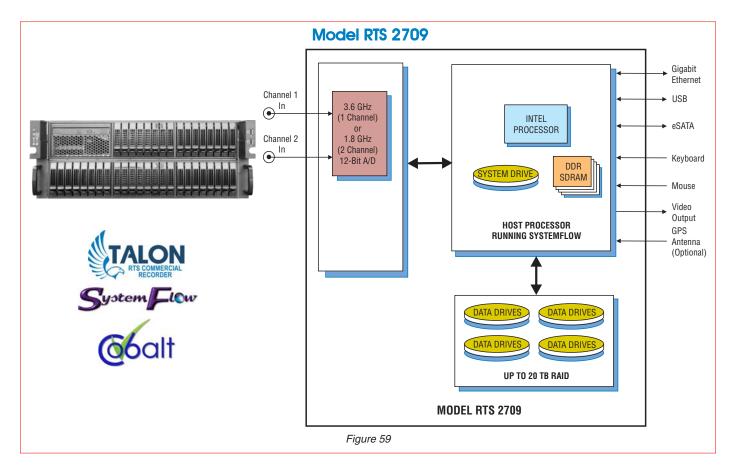
Included with the system is the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTS 2707 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2707 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2707 is configured in a 4U 19" rackmountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to increase channel counts and aggregate data rates.



## Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rackmount Recorder



The Talon RTS 2709 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2709 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3.2 GB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2709 uses Pentek's high-powered Virtex-6based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system.

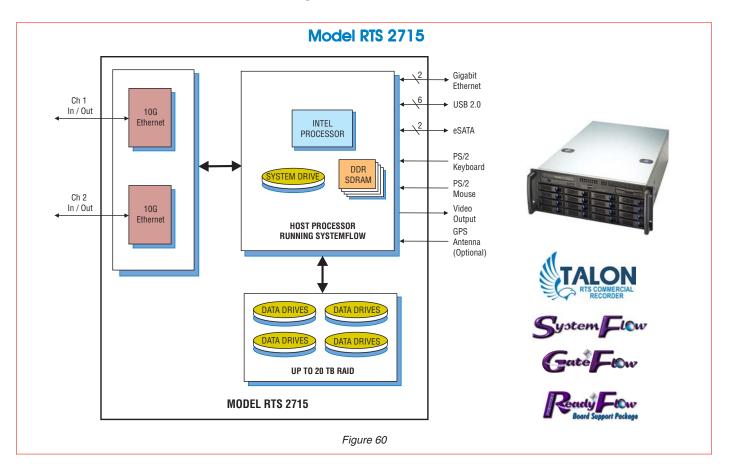
Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2709 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2709 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2709 records data to the native NTFS file system that provides immediate access to the data. The RTS 2709 is configured in a 4U 19" rackmountable chassis, with hotswap data drives, front panel USB ports and I/O connectors on the rear panel.





#### Two-Channel 10-Gigabit Ethernet Rackmount Recorder

The Talon RTS 2715 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highlyoptimized disk storage technology, the system achieves aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multimode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

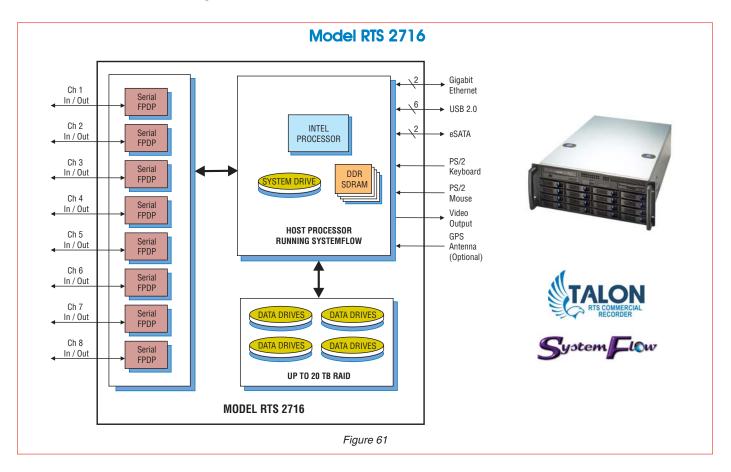
The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.





## Eight-Channel Serial FPDP Rackmount Recorder

The Talon RTS 2716 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.4 GB/sec.

The RTS 2716 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/ loop modes. The system is capable of handling 1.0625,

2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per serial FPDP link.

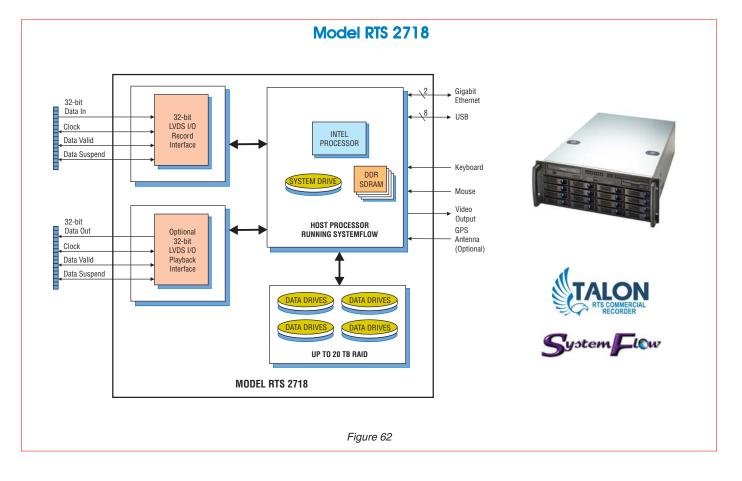
Built on a server-class Windows 7 Professional workstation, the RTS 2716 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2716 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2716 is configured in a 4U or 5U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Up to 24 hot-swappable SATA drives are optionally available, allowing up to 20 terabytes of real-time data storage space in a single chassis.

The RTS 2716 includes the SystemFlow Recording Software, which features a Windows-based GUI that provides a simple and intuitive means to configure and control the system.



## LVDS Digital I/O Rackmount Recorder



The Talon RTS 2718 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves sustained recording rates of up to 1 GB/sec.

The RTS 2718 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

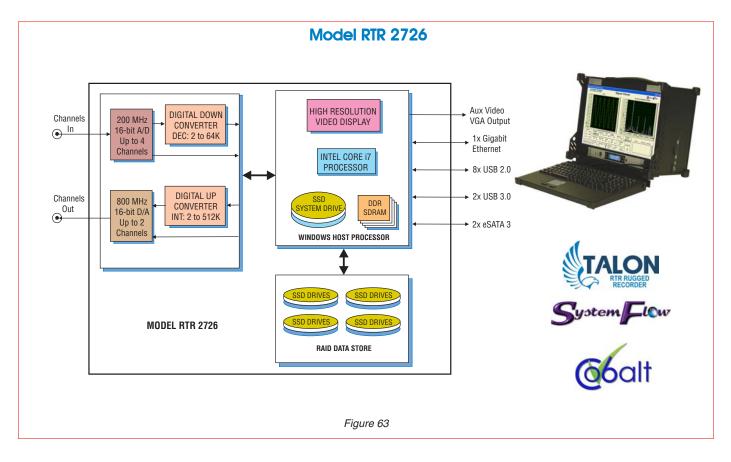
The RTS 2718 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. Built on a Windows 7 Professional workstation, the RTS 2718 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2718 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or eight USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD  $\pm$ R/RW drive.

The RTS 2718 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.



## Four-Channel RF/IF 200 MS/sec Rugged Portable Recorder



The Talon RTR 2726 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726 provides sustained recording rates of up to 1.6 GB/sec in a four-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726 is supplied in a small footprint portable package measuring just 16.9" W x 9.5" D x 13.4" H and weighing about 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

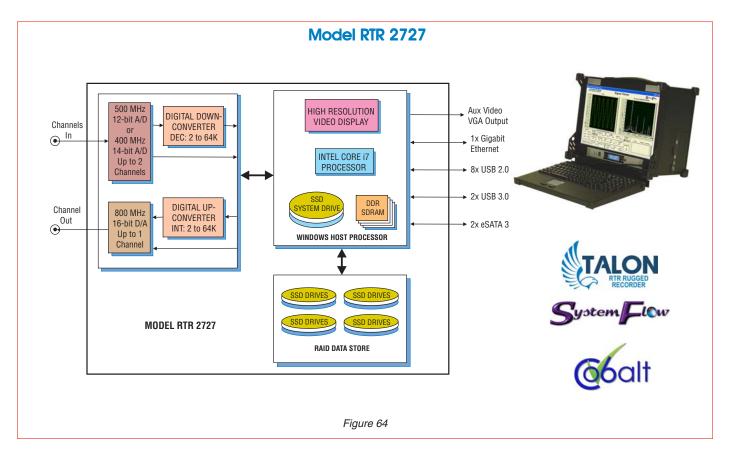
At the heart of the RTR 2726 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2726 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2726 performs well in ground, shipborne and airborne environments.



## Two-Channel RF/IF 500 MS/sec Rugged Portable Recorder



The Talon RTR 2727 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2727 provides sustained recording rates of up to 2.0 GB/sec in a two-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

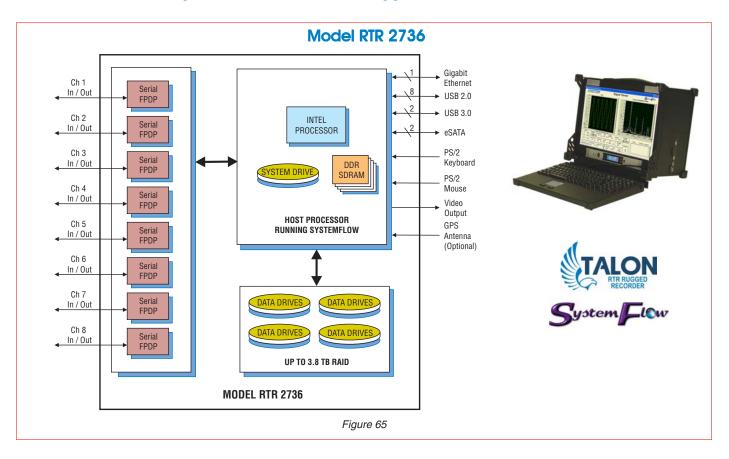
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At the heart of the RTR 2727 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2727 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2727 performs well in ground, shipborne and airborne environments.





## Eight-Channel Serial FPDP Rugged Portable Recorder

The Talon RTR 2736 is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

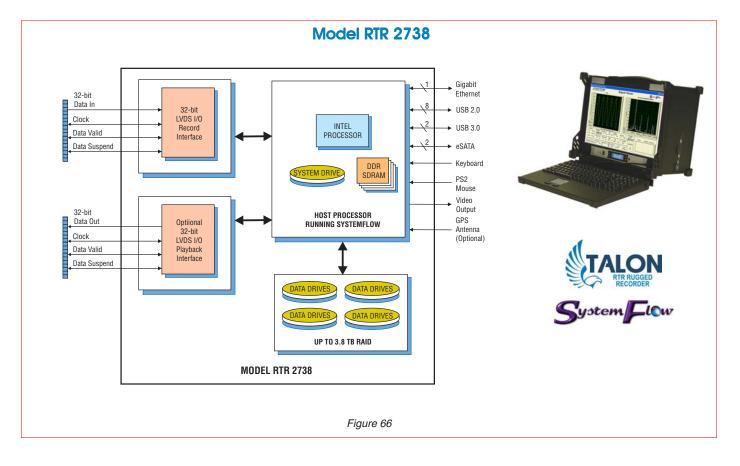
The RTR 2736 can be populated with up to eight SFP connectors supporting serial FPDP over copper, singlemode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 200 MB/sec per serial FPDP link. The RTR 2736 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2736 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide storage capacities of up to 3.8 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.



## LVDS Digital I/O Rugged Portable Recorder



The Talon RTR 2738 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the rugged, lightweight portable package achieves sustained recording rates of up to 1 GB/sec.

The RTR 2738 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity. Optional GPS time and position stamping accurately identifies each record in the file header.

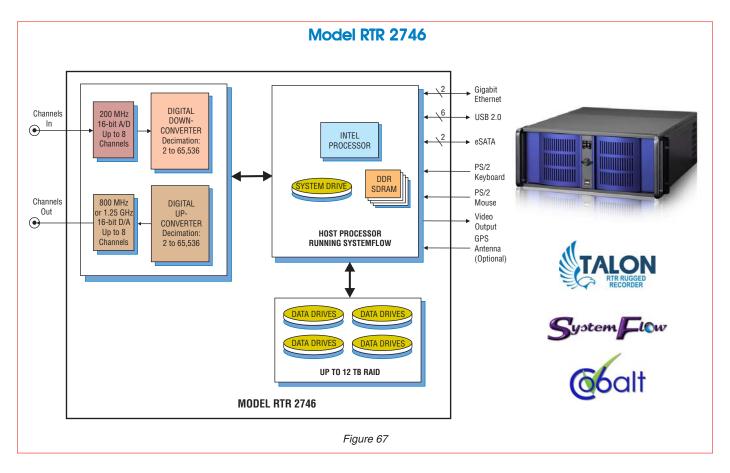
The RTR 2738 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. Built on a Windows 7 Professional workstation, the RTR 2738 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2738 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via a gigabit Ethernet port, eight USB 2.0 ports, two USB 3.0 ports or two eSATA 3 Ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD ±R/RW drive.

The RTR 2738 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impactresistant protective glass. Using shock- and vibrationresistant SSDs, the RTR 2738 is designed to reliably operate as a portable field instrument.



## Eight-Channel RF/IF 200 MS/Sec Rugged Rackmount Recorder



The Talon RTR 2746 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2746 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2746 can be configured to stream data to and from disk at rates as high as 2.0 GB/sec.

The RTR 2746 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz or 1.25 GHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system. The 24 hot-swappable SSD's provide storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2746 performs well in ground, shipborne and airborne environments.

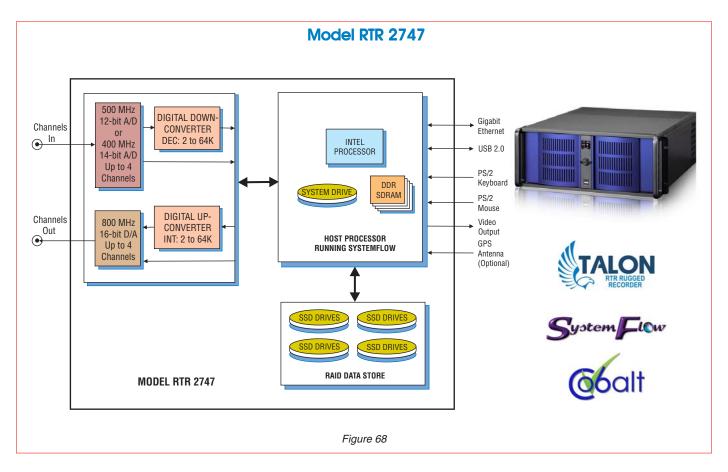
The RTR 2746 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.



## Four-Channel RF/IF 500 MS/Sec Rugged Rackmount Recorder



The Talon RTR 2747 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2747 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2747 can be configured to stream data to and from disk at rates as high as 4.0 GB/sec.

The RTR 2747 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system. The hot-swappable SSD's provide storage capacity of up to 11.5 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2747 performs well in ground, shipborne and airborne environments.

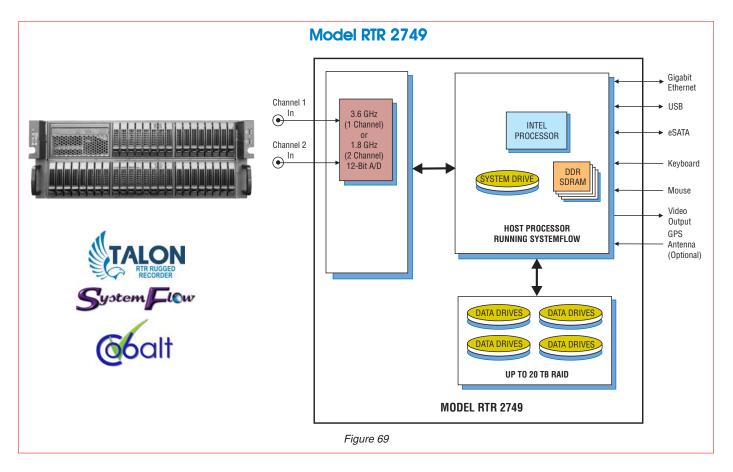
The RTR 2747 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.



## Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rugged Rackmount Recorder

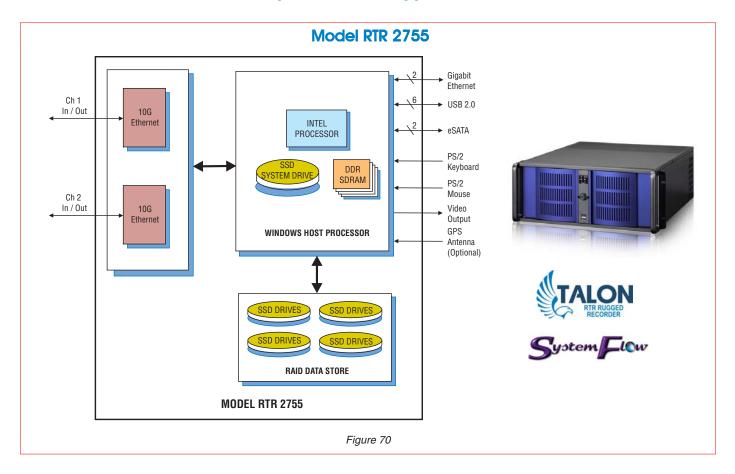


Designed to operate under conditions of shock and vibration, the Talon RTS 2749 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2749 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3,200 MB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2749 uses Pentek's high-powered Virtex-6based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system. Optional GPS time and position stamping allows the user to capture this information in the header of each data file. The RTS 2749 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2749 allows the user to install post processing and analysis tools to operate on the recorded data. The hot-swappable SSDs provide a storage capacity of up to 20 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2749 performs well in ground, shipborne and airborne environments.





## Two-Channel 10-Gigabit Ethernet Rugged Rackmount Recorder

Designed to operate under conditions of shock and vibration, the Talon RTR 2755 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized solid-state drive storage technology, the system guarantees loss-free performance at aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces.

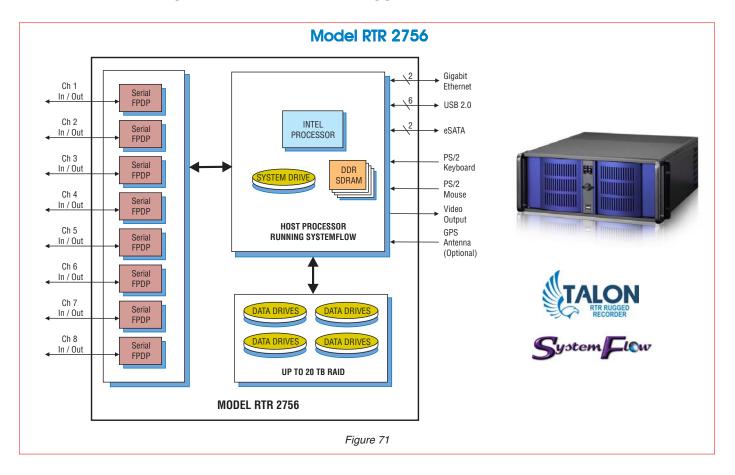
Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2755 includes the SystemFlow Recording Software that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2755 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2755 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2755 performs well in ground, shipborne and airborne environments. The 24 hotswappable SSD's provide a storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.





#### Eight-Channel Serial FPDP Rugged Rackmount Recorder

Designed to operate under conditions of shock and vibration, the Talon RTR 2756 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.4 GB/sec.

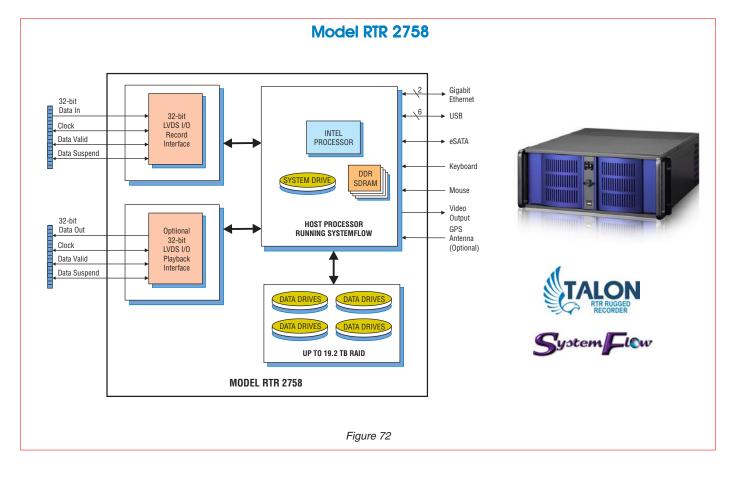
The RTR 2756 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per serial FPDP link. Built on a server-class Windows 7 Professional workstation, the RTR 2756 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2756 records data to the native NTFS file system, providing immediate access to the data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2756 performs well in ground, ship and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2756 can provide storage capacities of up to 19.2 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Multiple RAID levels, including 0,1,5, 6, 10 and 50 provide a choice for the required level on redundancy. Redundant power supplies are optionally available to provide a robust and reliable high-performance recording system.



## LVDS Digital I/O Rugged Rackmount Recorder



The Talon RTR 2758 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the rugged rackmount system achieves sustained recording rates up to 1 GB/sec.

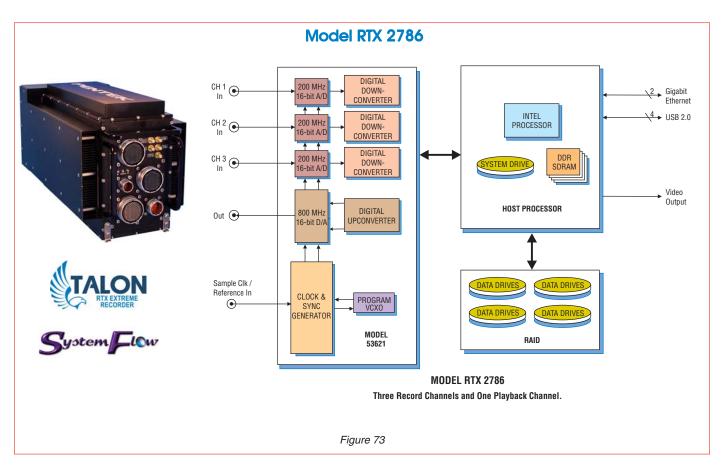
The RTR 2758 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2758 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. Built on a Windows 7 Professional workstation, the RTR 2758 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2758 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2758 performs well in ground, shipborne and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2758 can provide storage capacities of up to 19.2 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2758 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis that increase channel counts and aggregate data rates.





### Four-Channel RF/IF 200 MS/Sec Extreme 3U VPX Recorder

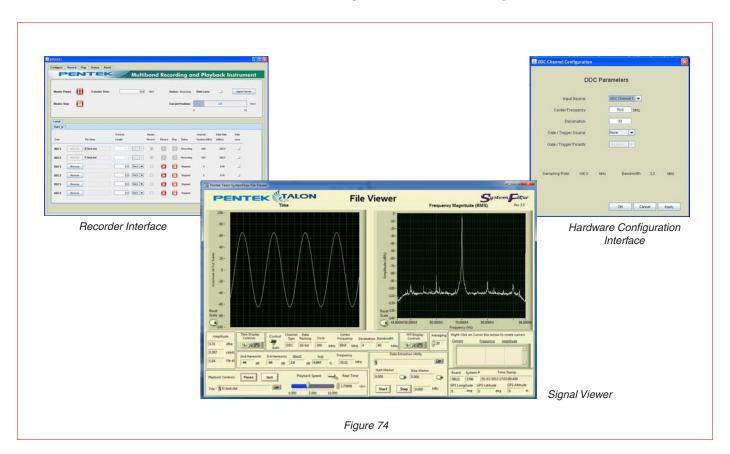
The Talon RTX 2786 is a turnkey, RF/IF signal recorder designed to operate under extreme environmental conditions. Housed in a ½ ATR chassis, the RTX 2786 leverages Pentek's 3U VPX SDR modules to provide a rugged recording system with up to four 16-bit, 200 MHz A/D converters with built-in digital downconversion capabilities. Optionally, the RTX 2786 provides one 800 MHz, 16-bit D/A converter with a digital upconverter for signal playback or waveform generation. As shown in the block diagram, the maximum number of record channels with this option is three.

The RTX 2786 uses conduction cooling to draw heat from the system components allowing it to operate in reduced air environments. It includes 1.92 TB of solid-state data storage, that allows it to operate with no degradation under conditions of extreme shock and vibration. The system is hermetically sealed and provides five D38999 connectors for power and I/O with four SMA connectors for analog I/O. The RTX 2786 includes Pentek's SystemFlow Recording Software. SystemFlow features a Windowsbased GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

The user API allows users to integrate the recorder as a subsystem of a larger system. The API is provided as a Ccallable library and allows for the recorder to be controlled over Ethernet, thus providing the ability to remotely control the recorder from a custom interface.

Four built-in solid-state drives provide reliable, high-speed storage with a total capacity of 1.92 TB.





#### Pentek SystemFlow Recording Software for Analog Recorders

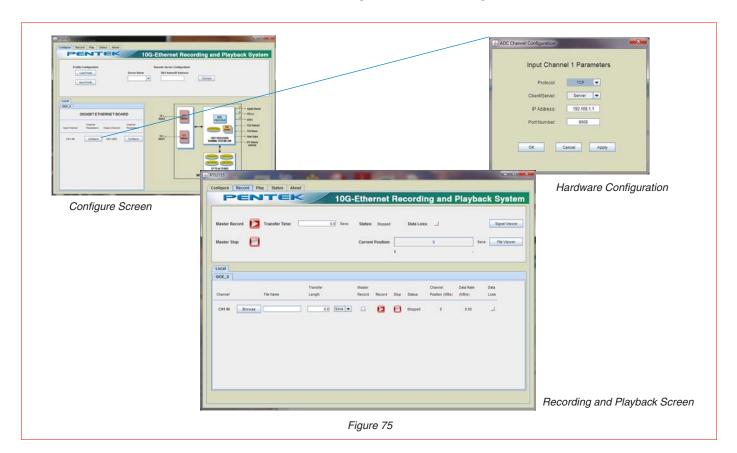
The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The Hardware Configuration Interface provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience. The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.





#### Pentek SystemFlow Recording Software for Digital Recorders

The SystemFlow Software for Digital Resorders provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators.

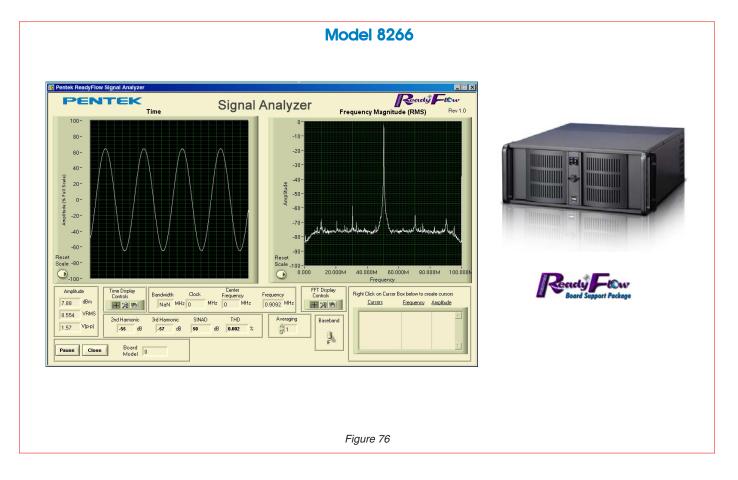
The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream. All parameters contain limit-checking and integrated help to provide an easier-touse out-of-the-box experience.

The **Configure Screen** shows a block diagram of the system, and presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. The **Recording and Playback Screen** allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a diskfull condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.



## PC Development System for PCIe Cobalt and Onyx Boards



The Model 8266 is a fully-integrated PC development system for Pentek 786xx Cobalt and 787xx Onyx PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

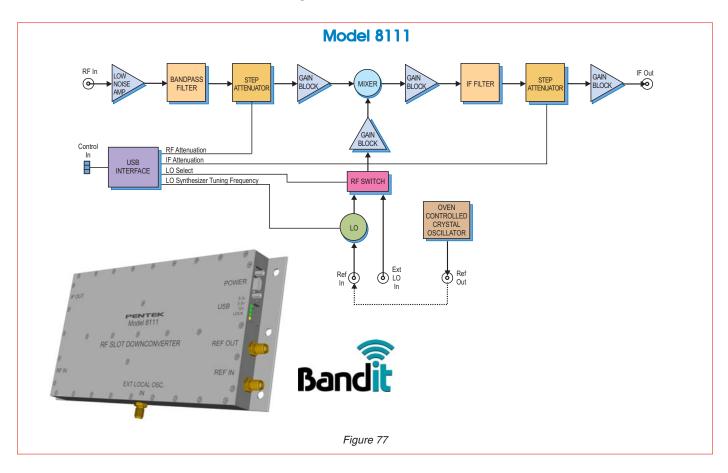
A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt and Onyx boards. A 1000-W power supply guarantees more than enough power for additional boards.





#### Bandit Modular Analog RF Slot Receivers and Downconverters

The Bandit<sup>®</sup> Model 8111 provides a series of high-performance, stand-alone RF slot receiver modules. Packaged in a small, shielded enclosure with connectors for easy integration into RF systems, the modules offer programmable gain, high dynamic range and a low noise figure. With input options to cover specific frequency bands of the RF spectrum, and an IF output optimized for A/D converters, the 8111 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

The 8111 accepts RF signals on a front panel SMA connector. An LNA (Low Noise-figure Amplifier) is provided along with two programmable attenuators allowing downconversion of input signals ranging from -60 dBm to -20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Seven different input-frequency band options are offered, each tunable across a 400 MHz band, with an overlap of 100 MHz between adjacent bands. As a group, these seven options accommodate RF input signals from 800 MHz to 3.000 GHz as follows:

Option	Frequency Band
001	800-1200 MHz
002	1100-1500 MHz
003	1400-1800 MHz
004	1700-2100 MHz
005	2000-2400 MHz
006	2300-2700 MHz
007	2600-3000 MHz

An 80 MHz wide IF output is provided at a 225 MHz center frequency. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.



# **Ruggedized Products**

## Levels of Ruggedization for High-speed VME/VXS, PMC/XMC, and OpenVPX Pentek Products

Level	LO	L1	L2	L3	L4
Cooling	Forced Air	Forced Air	Forced Air	Conduction	Conduction
Operating Temp	0° to 50°C	0° to 50°C	-20° to 65°C	-40° to 70°C	-40° to 85°C
Storage Temp	-20° to 70°C	-40° to 100°C	-40° to 100°C	-50° to 100°C	-50° to 100°C
Sine Vibration	-	2g 20-500 Hz	2g 20-500 Hz	10g 20-2000 Hz	10g 20-2000 Hz
Random Vibration	-	0.01 g <sup>2</sup> /Hz 20-2000 Hz	0.04 g <sup>2</sup> /Hz 20-2000 Hz	0.1 g <sup>2</sup> /Hz 20-2000 Hz	0.1 g <sup>2</sup> /Hz 20-2000 Hz
Shock	-	10g, 11 ms	20g, 11 ms	<mark>30g</mark> , 11 ms	40g, 11 ms
Humidity* No Conf Coat	0% to 95%	0% to 95%	0% to 95%	<mark>0%</mark> to 95%	0% to 95%
With Conf Coat	0% to 100%	0% to 100%	0% to 100%	<mark>0% to</mark> 100%	0% to 100%
* non-condensing Figure 78					

To make Pentek's high-speed VME/VXS, PMC/ XMC and OpenVPX products operate in harsh environments of heat, vibration, shock or altitude, five different levels of ruggedization are offered.

This chart shows the five levels and the appropriate environmental specifications for each.

Level L0 is standard commercial level for normal laboratory environments.

Levels L1 and L2 are for forced air cooling environments where temperature, shock and vibration may be a factor. Examples of such environments are shipboard installations and military vehicles.

Levels L3 and L4 are provided for environments where air in not available to cool the boards. This could be due to very high altitudes or severe conditions of dust, moisture or sand.

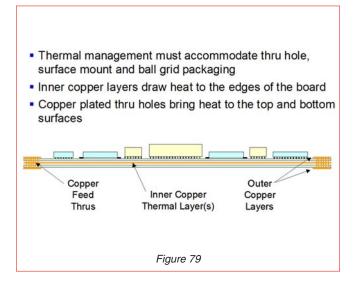
Instead, the boards are put in a sealed enclosure and heat is drawn out through thermal conduction.

In the next few pages we illustrate our strategy for conduction cooling.



# **Ruggedized Products**

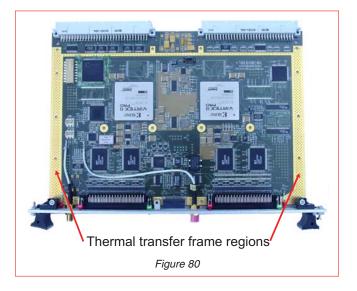
## Conduction Cooled Printed Circuit Board Design



The printed circuit board is manufactured with layers of heavy copper planes to pull heat out to the edges of the board.

Feedthrough holes are stitched along the edges to bring the heat to the top and bottom surfaces.

## Commercial LO Model 6821 Showing Thermal Transfer Pads



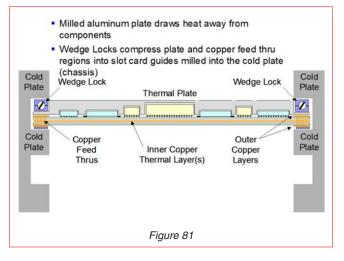
This shows the commercial version of the board which does not have the conduction cooling hardware installed.

Note the provisions for the thermal transfer regions along both edges that come into play for the conduction cooled version.



# **Ruggedized Products**

#### Conduction Cooling Mechanical Hardware



For conduction cooling, an aluminum thermal plate is milled to conform to the various heights of each component.

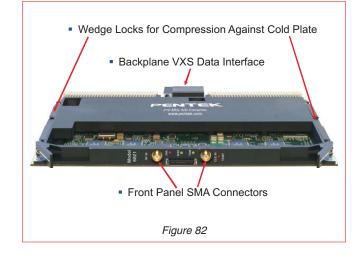
It conducts heat away from the components and towards the left and right edges of the board.

A wedge lock compresses the plate and the copper feedthrough regions into slots of the aluminum chassis cardguide to ensure good thermal contact with the slot.

Heat flows through the aluminum thermal plate and copper layers into the slots in cold plates forming the sides of the chassis.

The cold plate must be maintained below a maximum temperature by a heat exchanger or some other external cooling method.

#### L3 Conduction Cooled Version of Model 6821

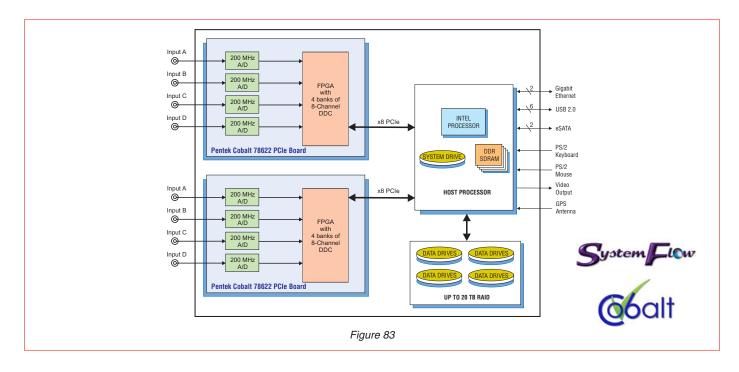


Here's a photo of the L3 conduction cooled version of the Model 6821 A/D Converter.

Also, notice the VXS P0 connector in the middle of the back edge of the board.

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#### 64-Channel Software Radio Recording System

Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. All of the 8 channels within each bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8*f_s/N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of  $f_s/N$ . Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

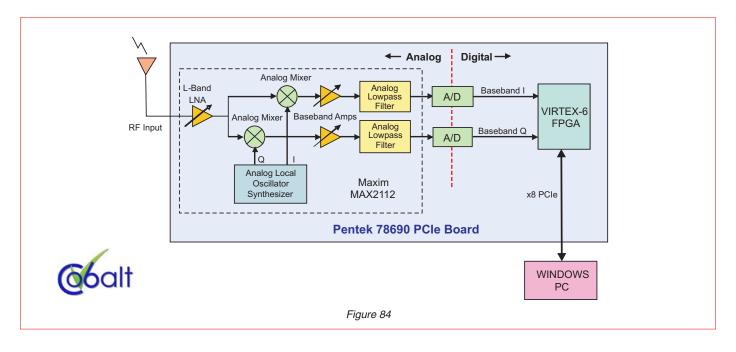
An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An onboard clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel® Core<sup>TM</sup> i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.







The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

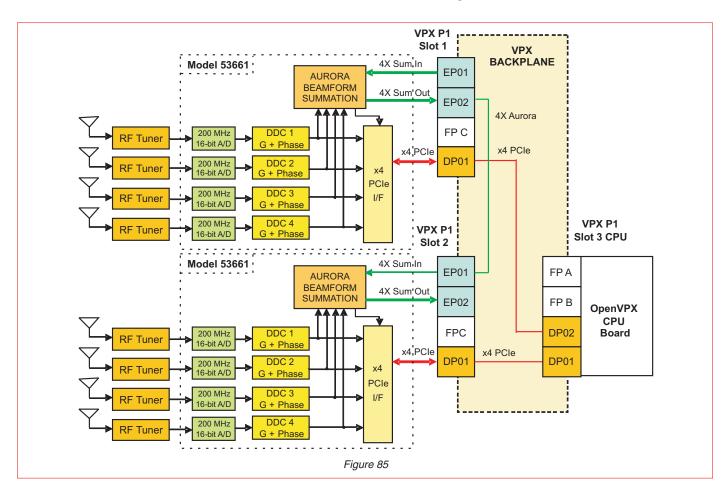
The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz. The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs. The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size adderesses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.





### 8-Channel OpenVPX Beamforming System

Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

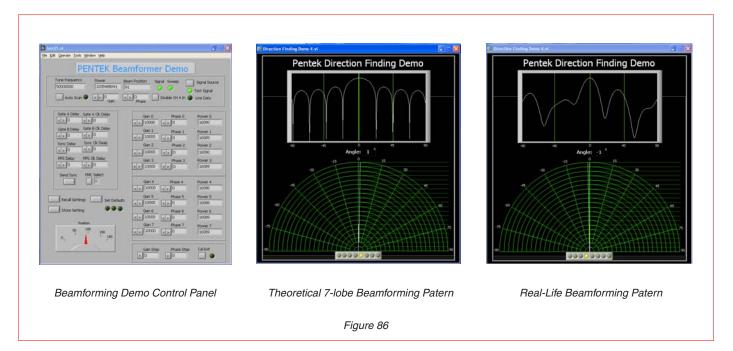
The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX "fat pipes". The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. >





#### 8-Channel OpenVPX Beamforming Demo system

➤ The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum sensitivity across arrival angles from  $-90^{\circ}$  to  $+90^{\circ}$  perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0° angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link: <u>Beamforming Demo.</u>



# Summary

## Summary



As we have seen, quite a bit of technology needs to surround and support these new high-speed A/D converters in order to deploy them successfully in realtime systems.

A complete signal acquisition plan must be developed. It should include frequency content of the signal, voltage levels, accuracy, and bandwidth.

Processing these extremely high-speed sample streams is often possible only with FPGA technology.

FPGAs can also help implement interfaces to switched serial fabrics so that data can be successfully delivered to other parts of the system.

We looked at several product examples and then at some applications that illustrate the impressive variety of tasks and systems made possible by this technology. For more information on the Pentek products described in this handbook, use the links provided in the following pages.

## For More Information....



Here's a list of useful links you can use to check out more details about the manufacturers' devices used in the products we have discussed.

For specifications for VXS and XMC, the switched fabric for PMC, visit the VITA (VMEbus International Trade Organization) website.

You can also learn more about the switched serial fabric standards and protocols from the respective trade and technical organizations for each of them.





The following links provide you with additional information about the Pentek products presented in this handbook: just click on the model number. Links are also provided to other handbooks or catalogs that may be of interest to you in your development projects.

Model	Description	Page
6821	215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS	19
6822	Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS	20
6826	Dual 2 GHz, 10-bit A/D with Virtex-II FPGA - VME/VXS	21
7142	Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC	22
7242	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI	22
7342	Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI	22
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI	22
7742	Multichannel Transceiver with Virtex-4 FPGAs - Full-length PCIe	22
7842	Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe	22
5342	Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX	22
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC	23
7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 6U cPCI	23
7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U cPCI	23
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI	23
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length PCIe	23
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length PCIe	23
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX	23
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