New!

Model 7811

Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

General Information

Model 7811 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to serial FPDP data converter boards or as a chassis-to-chassis data link.

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 7811 serves as a flexible platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 7811 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

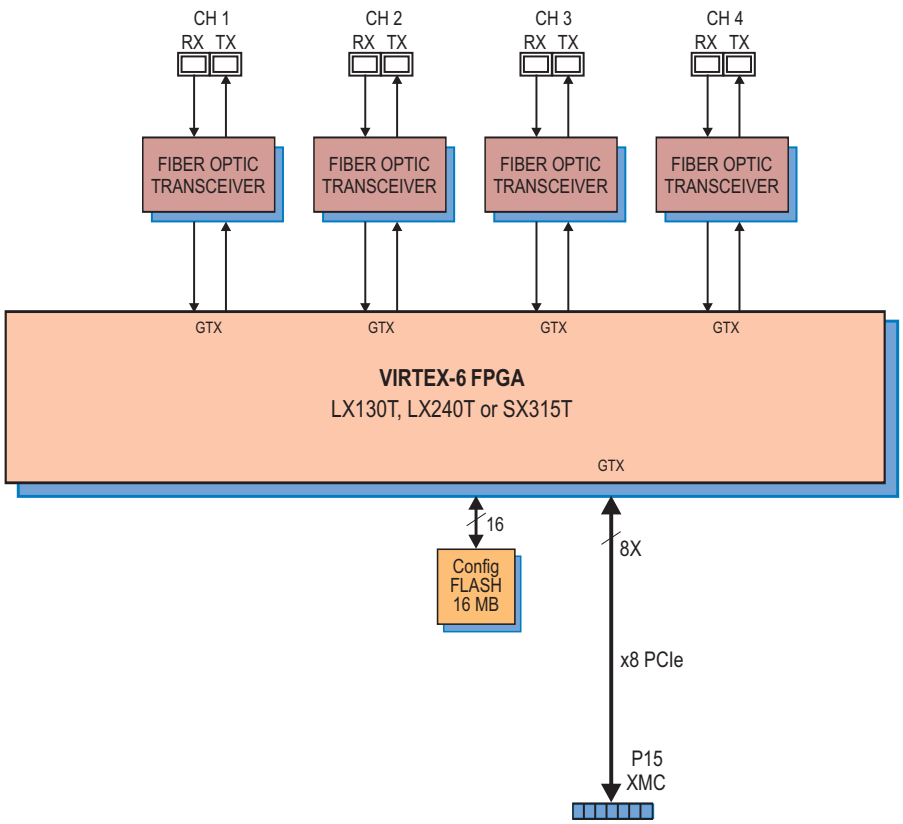
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T or LX240T. The LX240T part features 768 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LX130T FPGA can be installed. ➤

Features

- Complete serial FPDP solution
- Fully compliant with VITA 17.1specification
- PCI Express interface up to x8



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Model 7811 — Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

➤ Serial FPDP Interface

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0635, 2.125 and 2.5 Gbaud link rates and the option for multi-mode and single-mode optical interfaces or copper interfaces the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

PCI Express Interface

The Model 7811 includes an industry-standard interface fully compliant with PCI Express bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four sFPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- **Number of Connectors:** 4
- **Connector Type:** SFP, optical or copper
- **Optical Connector Type:** LC
- **Optical Laser:** 850 nm (standard, other options available)

Link Rates: 1.0635, 2.125 or 2.5 Gbaud

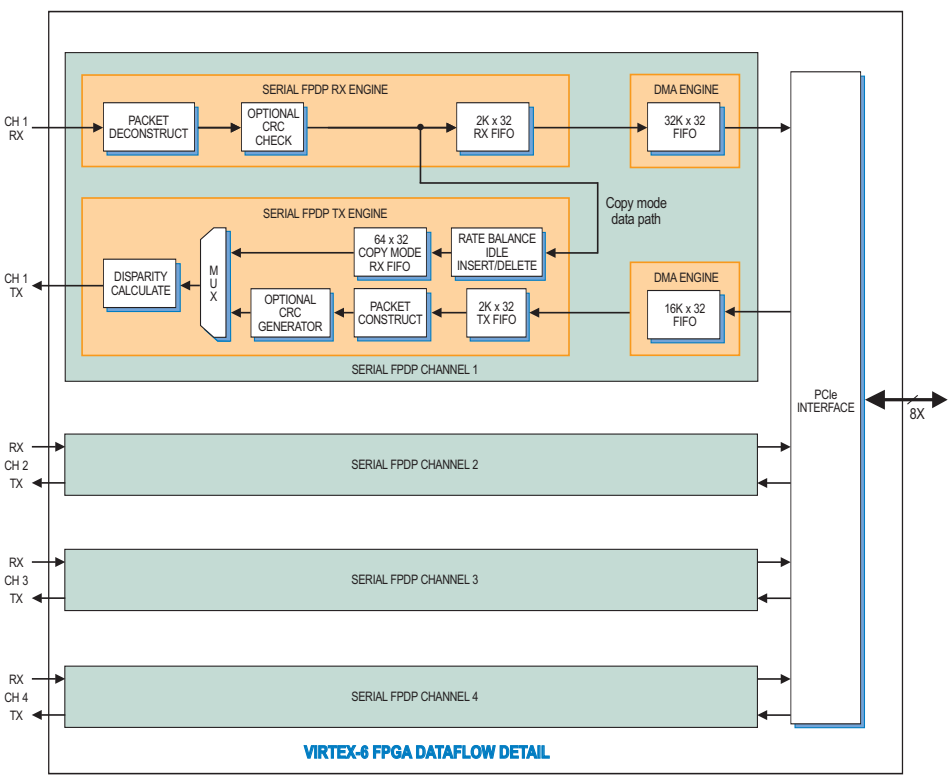
Data Transfer Rates: 85, 170 or 200 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in. ➤



Ordering Information

Model	Description
7811	Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe
Options:	
-062	XC6VLX240T FPGA

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➤ Serial FPDP VITA 17.1 Compliance

The 7811 fully complies with the VITA 17.1 specification as follows:

What Link Rate does the interface support?
■ 1.0625 Gbaud ■ 2.125 Gbaud ■ 2.5 Gbaud

What Serial FPDP function does the interface support?
__ Transmitter only __ Receiver only ■ Transmitter & Receiver

Does the Receiver support Flow Control (setting the STOP signal)?
__ Always active __Not supported ■ Optional (selectable)

Does the Transmitter support Flow Control (stopping data transmission on receipt of a STOP signal)?
__ Always active __ Not supported ■ Optional (selectable)

If the Transmitter supports Flow Control, after transmitting a STOP signal, how many 32-bit words can be received before a Receive FIFO overflow occurs?
■ Programmable

Does the interface support CRC?
__ Always active __ Not supported ■ Optional (selectable)

Does the Transmitter support Copy Master Mode (insertion of additional IDLE ordered sets)?
__ Always active __ Not supported ■ Optional (selectable)

Does the Receiver support Copy Mode (re-transmission of data)?
■ Yes __ No

If Copy Mode is supported, what method is used for implementation (see VITA 17.1 Observation 6.1.4.4)?
__ Method 1 ■ Method 2

Does the Receiver support Copy/Loop Mode (re-transmission of data and setting Flow Control)?
■ Yes __ No

What type of media is supported?
■ Short Wave Laser ■ Long Wave Laser ■ Copper

What type of media connectors are supported?
■ LC __ SC __ ST __ HSSDC/HSSDC-2 ■ RJ-45

Which fiber transmit data frames are supported in addition to Normal Data Fiber Frames (see VITA 17.1 Permission 7.3.3.1)?
__ Sync without Data Fiber Frames ■ Sync with Data Fiber Frames

Does the Serial FPDP Transmitter stop in response to the Serial FPDP Receiver sending NRDY True (see VITA 17.1 Observation 7.3.2.2)?
__ Always __ Never ■ Optional (selectable)

Are status bits kept up to date when there is no data to transmit by sending empty Serial FPDP Normal Data Fiber (see VITA 17.1 Rule 7.3.3.8, Recommendation 7.3.3.2 and Suggestion 7.3.3.1)?
■ Yes, empty frames transmitted __ No, status is not updated when no data is transmitted