Data Transmission Test Set

Model 650

Features

- **1 bps to 36 Mbps Operation (Standard)**
  1 bps to 50 Mbps Operation (Optional)
- **Independent Transmitter and Receiver**
- **Measures: Bits, Seconds, Bits in Error, Seconds in Error, Bit Error Rate (instantaneous and average)**
- **Data Symmetry & Bit Slip Tests**
- **TX & RX Frequency Measurement**
- **16 PRN Sequence Codes Forward & Reverse 2^n-1, n= 5, 7, 9, 11, 15, 20, 23, 31 (Forward or Reverse) and User Defined Taps on 31-bit Register.**
- **Fixed Programmable Data Patterns 8, 16, 32, 64, 128, 256-bit or Dotting**
- **Internal DDS Frequency Synthesizer**
- **IRIG Code Generation and Conversion**
- **Randomizer / Derandomizer**
- **IRIG, V.35, V.36**
- **Convolution Encode / Decode (Optional)**
- **TTL, Bipolar, RS-422 Signal Interfaces**
- **Remote Control / Monitor: RS232 (Standard)**
  EtherNet, IEEE-488 (Optional)
- **Internal Noise Source (Optional)**
  Programmable Eb/No and Signal Level
- **Analog Signal Output Interface (Optional)**
- **Acquisition Time Test (Optional)**
- **Jitter Test (Optional)**
- **3½" Rack Mount Chassis**

Functional Description

A modular architecture gives the Model 650 superior flexibility. A fully programmable frequency synthesizer allows transmit clock generation from 1 bps to 50 Mbps with 6-digit resolution. A flexible interface structure, which provides IRIG code converters for both input and output data, allows the Model 650 to fully support test and evaluation of telemetry receive, and processing systems.

The BER (Bit Error Rate) Module, is the major functional element in the Model 650. A microprocessor resident on the BER module controls the BERT transmit and receive circuits through user commands issued from the local front panel or remote control port. Communication between the microprocessor module and the BER module is accomplished using semaphores passed into a dual-port RAM architecture.

All high-speed functions are provided by hardware Functions such as data generation, PRN correlation, error detection and accumulation are performed by hardware. Low speed functions, such as test data accumulation and formatting for the front panel and remote monitoring ports, are provided by the embedded microprocessors.

Data Link Testing up to 50 Mbps

General Description

The GDP Model 650 Data Transmission Test Set fills the need for high performance data-link verification and qualification at an affordable price. The user is provided with totally independent transmit and receive functions to allow rapid fault isolation and data link characterization. Simulated signal perturbations are created in the test lab by adding noise, baseline offset and varying signal levels. Features such as an internal 6-digit frequency synthesizer and IRIG Code generator and converter make the Model 650 especially suited to the test and evaluation of PCM Telemetry data link systems and components.

The Model 650 provides measurement capability for: Accumulated Bit Errors, Measured Bit Error Rate, Elapsed Test Time, Accumulated Errored Seconds, Errors per Second, Measured error Symmetry, Accumulated Bit Count Integrity loss (Bit Slips), Measured Transmit and Receive clock rate.

Operating ease and test flexibility is the result of using microprocessor control to augment high speed hardware functions. A high contrast vacuum fluorescent display provides setup and test result information in easy-to-use formats.

Applications

DATA LINK TESTING

In a telemetry ground station or in a satellite ground data handling system, the Model 650 provides the capability to perform data-link quality analysis and overall system checkout. A single Model 650 provides independent data transmit and data receive circuits to support loop-back verification of a ground station.

The Model 650 is user programmed for a particular data pattern and bit rate. By utilizing appropriate connection points in the communications system, the entire data link is tested from antenna through bit synchronizer. Recovered data is synchronized by the Model 650 and test results are accumulated for user analysis.

BIT SYNCHRONIZER TESTING

The Model 650 provides high performance functionality and ease-of-use in a single package. Using the internal (option) or external noise source with the adjustable Eb/No setup, greatly simplifies Bit Sync Testing. These features coupled with the GDP VI Software make the Model 650 an excellent addition to any telemetry system or Bit Synchronizer Test Station.

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Data Transmission Test Set

Model 650

SPECIFICATIONS

GENERAL

Operation:
- Independent Transmitter and Receiver
- 1 bps to 36 Mbps NRZ codes
  (17.5 Mbps for 2X codes) Standard
- 1 bps to 50 Mbps NRZ codes
  (30 Mbps for 2X codes) Optional
- TTL-50 Mbps, Bipolar-40 Mbps, RS-422-40 Mbps
  Frequency Display:
- Receive and Transmit, measured

Input Termination:
- High Z / Low-Z on TTL & Bipolar

Data Pattern Selectable:
- Forward and Reverse PRN codes:
  2^5-1, 2^7-1, 2^9-1, 2^{11}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, 2^{31}-1, User selectable Taps
- Recycle data patterns, programmable
  8, 16, 24, 32, 64, 128, 256 bits or Dotting
- IRIG Bit-Codes:
  NRZ-L/M/S; BiØ-L/M/S; DM-M/S

Data Randomizer / Derandomizer:
- V.35, V.36 or IRIG (n=15) RNRZ-L

Convolutional Encoder (Viterbi Decoder) (Option):
- Rate ½ ; K 7
- Selectable convolution order and polarity

TRANSMITTER

Data/Clock Outputs:
- Transmit I-and Q (Option)-Data
- Transmit Clock

Clock Input:
- External Transmit Clock - Selectable

Transmit Timing:
- Internal Frequency Synthesizer
- Six (6) digit-plus-exponent

Data Perturbations:
- Force output ALL 1s or ALL 0s
- Insert a single error
- Insert a single slip
- Insert bit-error-rates from 1.0E-06 to 0.5
- Insert Gap
- Selectable data slip up to 9999 bit times
- Selectable data gap up to 9999 bit times
- Bit Rate Jitter (Option)
- AC Base-line Variation (w/ Analog Option)
- Signal Amplitude Modulation (w/ Analog Option)

RECEIVER

Receive Data and Clock, Synchronization:
- Auto Polarity Correction
- Auto-correlation BER up to 3 x 10^{-1}.
- ReSynch Threshold, Selectable
- Error Allowance Threshold

Tests:
- Test length from 10^2 thru 10^{12} bits
- Total Count since test start:
  Bits, Bits-in-Error, Seconds, Errored-Seconds, Slips
- Calculations:
  Bit-Error Rate, Symmetry, Average Bit-Error Rate
- Sync Acquisition (Option)

ANALOG INTERFACE (option)

Transmit Data with level and offset adjust:
- Signal level: 100 mV_{p-p} to 4 V_{p-p} (50 Ω Load)
- DC offset: Up to +5V or - 5V (Peak signal + Offset + Noise)

Noise: (Option)
- Internal programmable Eb/No generator
- External Noise Input

LOCAL front panel CONTROL

- Power ON/OFF
- Display and Keypad
- Soft Control Keys
- LED Status and Test Points

MISCELLANEOUS

AC Input:
- 90 to 264 VAC Auto-set
- Single Phase, 47-63 Hz

Size:
- 3.5 (H) x 20 (D) x 17 (W), inches

Weight: 20 lbs.

Mounting: 19 inch EIA rack mount

Environment, Operating:
- Temperature: 0 to 40° C
- Relative Humidity: 5 to 95%, no condensation
- Altitude: 0 to 10,000 ft
- Forced-air Cooling

REMOTE CONTROL

- RS-232 Serial Interface (Std)
- IEEE488 Interface (Optional)
- Ethernet - 10/100 Base T (Optional)

Ordering Information

2100215

MD650-00	Base Unit	OP650-65	Internal Noise Source
OP650-21	IEEE Remote Control	OP650-66	Sync Acquisition Test
OP650-22	Ethernet Remote Control	OP650-70	75 Ohm I/O Impedance
OP650-40	Special I/O	OP650-89	Chassis Slides
OP650-62	Extended Bit Rate 36 to 50 Mbps	OP650-VI	Virtual Interface Software

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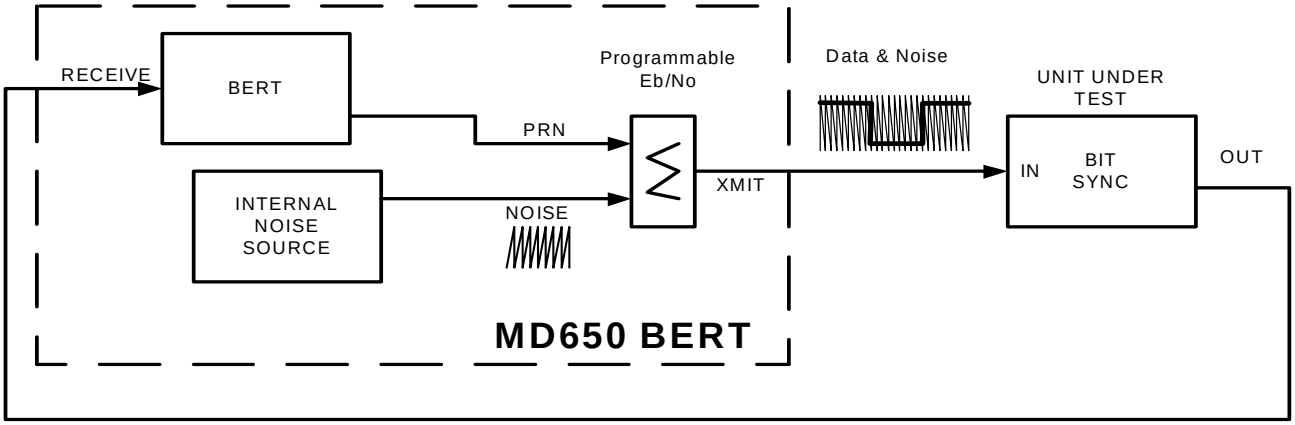
Model 650 Option: Internal Noise Source

OP650-65

OP650-65: Data Link Analyzer Internal Noise Option



Including Noise and Analog output functionality in the Model 650 adds a layer of capability that allows testing of bit synchronizers and data links to a higher level. Real-World performance of a system is more fully characterized under the test conditions provided by this option.

SPECIFICATIONS

Noise:

- White Gaussian Noise
- Eb/No (Programmable): -3 dB to 15.9 dB (0.1 dB increments)
- Automatic Eb/No Settings from Front Panel (No Calculations or Measuring Required)
- Absolute Accuracy: Better than ±0.5 dB (0.1 dB typical)
- All Digital Design
- Repeatable Results
- Easy Bit Synchronizer BER Testing to IRIG106 Theoretical Curves

Output Level:

- 0 to 4 Vp-p into 50 Ohms
  - * Adjustable Output Signal Level: 0.1 Vpp Steps
- Fixed or AM Modulated Output Signal Level
  - * Amplitude Modulation Level: 0 to 100% of Peak Signal
  - * Amplitude Modulation Frequency: 0 to 0.1% of Bit Rate in 0.01% Steps

Baseline Offset:

- Adjustable Static Offset Level: ± 100% Peek Signal Level
- Adjustable Dynamic Offset Rate : 0 to 0.1% of Bit Rate (0.01% Resolution)

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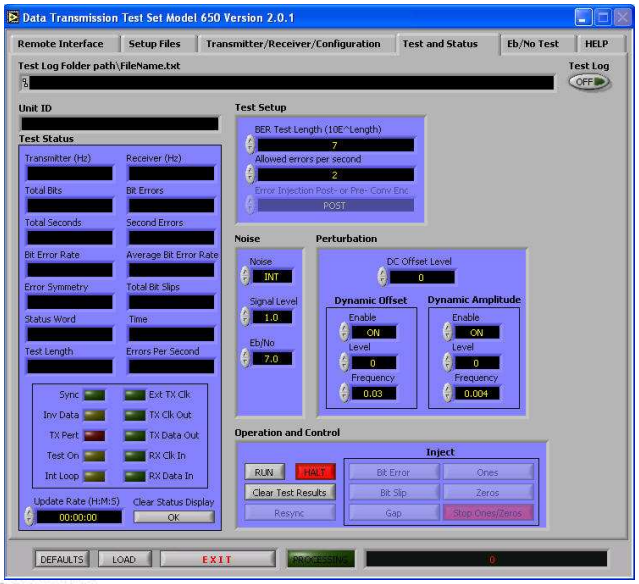
Model 650 Option: Virtual Interface Software

OP650-VI

The Virtual Interface (VI) Software for the Model 650 provides an easy to use intuitive Graphic User Interface on a personal computer.

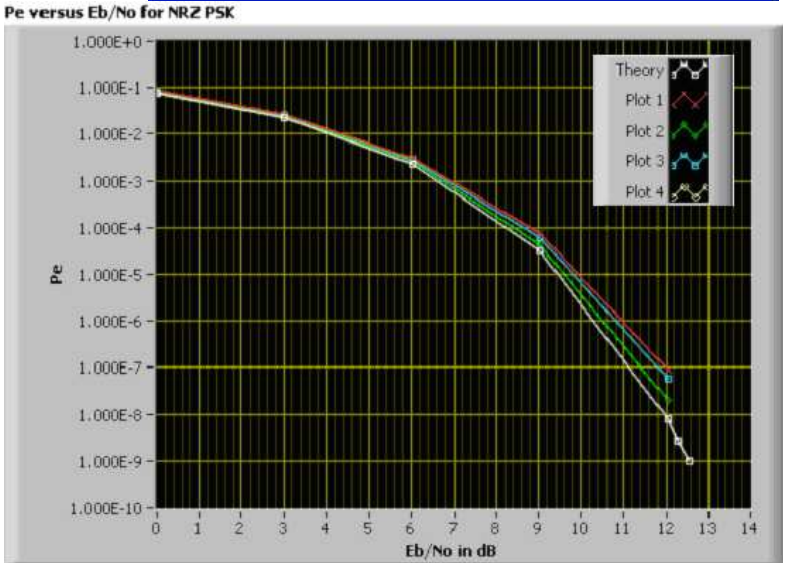
All operational parameters needed to control the Model 650 to accomplish a test are entered into easily understood dialog windows. Once all parameter settings are made, a simple click of a button transfers all setup information to the BERT.

All remote control interfaces, which are available on the Model 650 are supported by the VI. Complex system arrangements consisting of multiple components, provided by GDP Space Systems, are controlled using the bussable interface structures (IEEE-488 or Ethernet) and the appropriate VI software for each unit.



Test results are gathered by the OP650-VI software and presented in a format easily interpreted by the user. A test result log-file may be designated by the user into which all accumulated test result data is stored for use by other software. This data file is recorded as ASCII, comma delimited information making it useful for direct inclusion in written reports.

If the Model 650 includes the Noise option (OP650-65), automatic bit synchronizer and data link testing is made possible, which results in a complete family of noise performance curves. The time consuming task of calculating values of noise and signal levels as well as making settings to filters is automatically performed by the Model 650. The OP650-VI takes full advantage of the features of the Model 650 to provide highly understandable and comprehensive test results.



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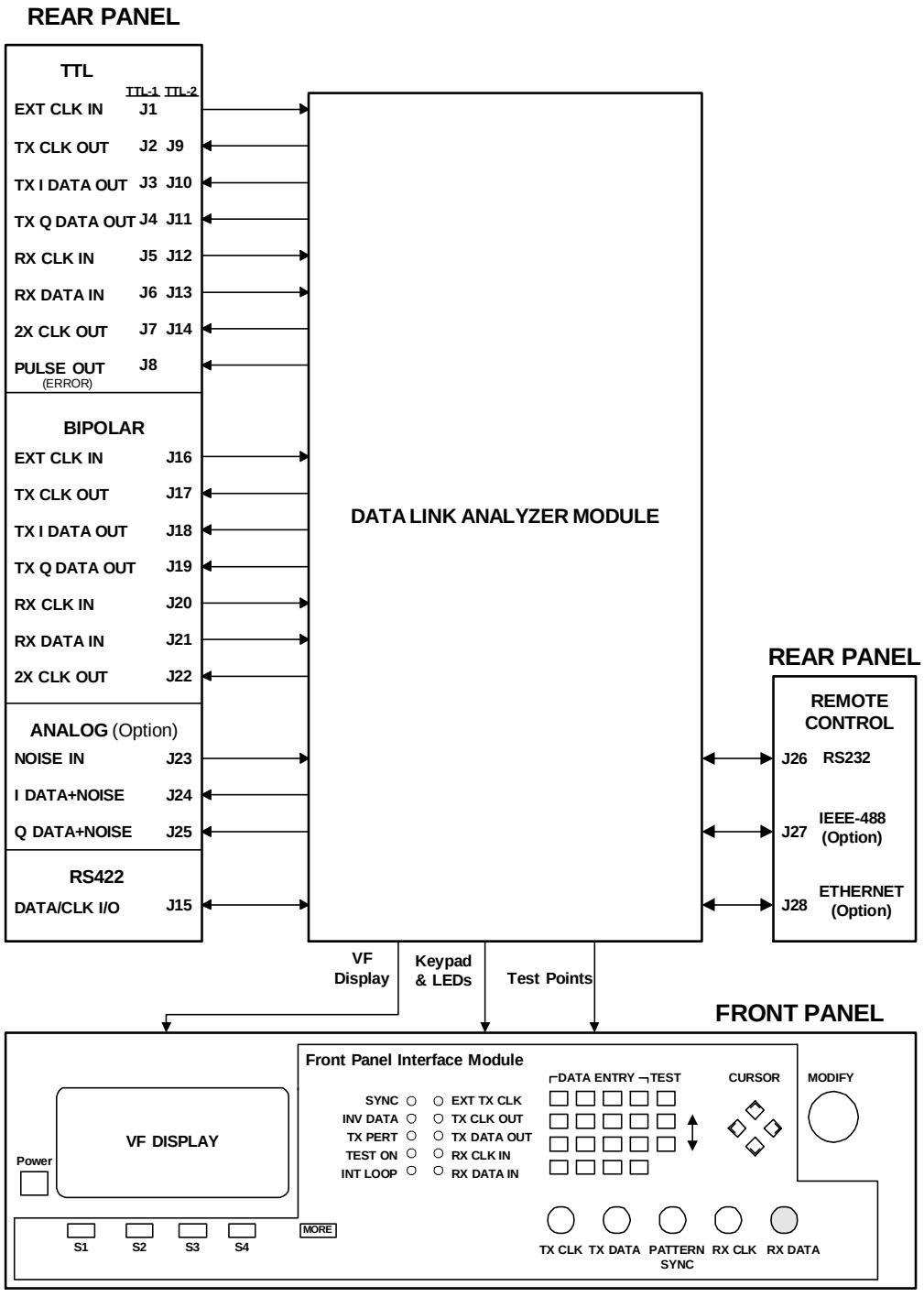

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