

New!

FlexorSet Model 5973-317

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX



Features

- Supports Xilinx Virtex-7 VXT FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-317 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 5973-317 includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-317 includes factory-installed applications ideally matched to the board's

analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

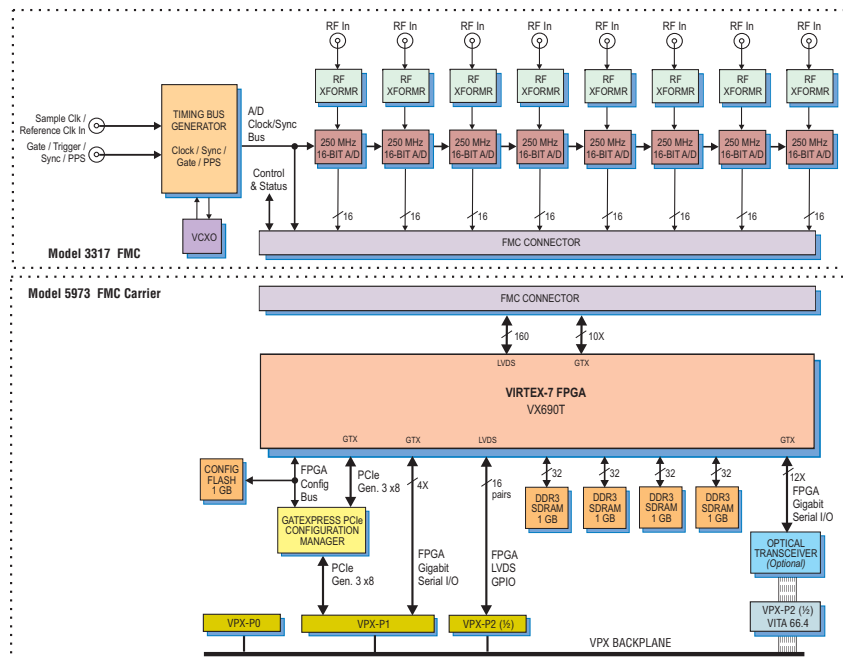
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. ▶



► Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.

A/D Acquisition IP Modules

The 5973-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 * f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

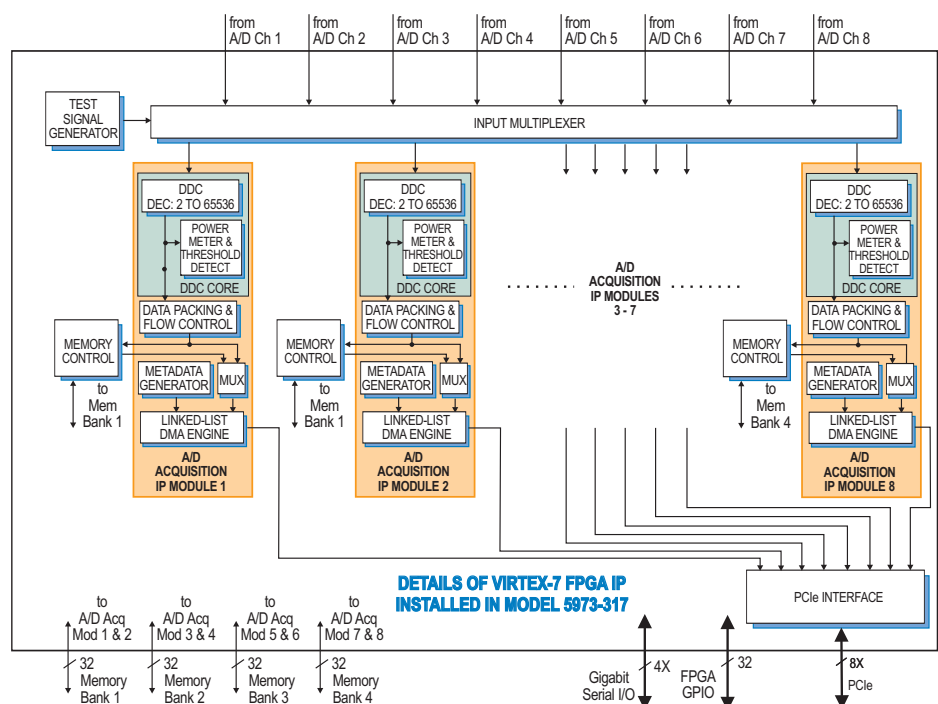
GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. ►



Memory Resources

The 5973-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5973-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



Ordering Information

Model	Description
5973-317	8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:

-104	LVDS FPGA I/O to VPX P2
-110	VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

► In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC46TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Eight channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)