New!

Model 3316

8-Channel 250 MHz, 16-bit A/D - FMC

FlexorReady Flow Board Support Package

Features

- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX Virtex-7 FMC carrier board
- Ruggedized and conduction-cooled versions available

General Information

The Flexor™ Model 3316 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems. When combined with the Model 5973 3U VPX Virtex-7 Processor and FMC Carrier, the board set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized to create larger multiboard systems.

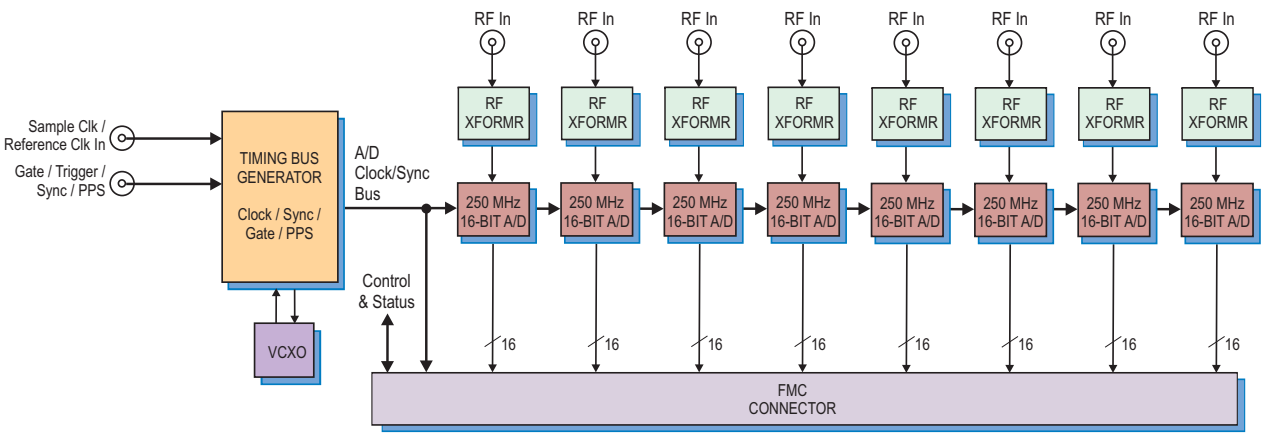
FMC Interface

The Model 3316 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3316 and the FMC carrier.

Unlocking the True Performance of the Model 3316

The Model 3316 is shipped with a simple Xilinx Vivado project for operating the FMC with the Xilinx VC707 Evaluation Kit. This project includes IP for initializing the FMC and confirming data paths, providing the user with a tested platform for creating their own FPGA IP for operating the FMC.

While users will find the Model 3316 an excellent analog interface to the VC707 or any compatible FMC carrier, the true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 FMC carrier. With factory installed IP, the board set provides a turnkey data acquisition subsystem, eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition engines, programmable digital downconverters, programmable linked-list DMA engines, and a metadata-packet creator. ➤



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8-Channel 250 MHz, 16-bit A/D - FMC

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

Model	Description
3316	8-Channel 250 MHz, 16-bit A/D - FMC

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

Model 5973/3316 A/D Acquisition IP Modules

The 5973/3316 board-set features eight A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the 5973 for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the 5973's PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor's job of identifying and executing on the data.

Model 5973/3316 DDCs (Digital Downconverters)

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D acquisition IP modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 256 providing a wide range to satisfy most applications.

ReadyFlow Board Support Package

When used with the 5973, Pentek's ReadyFlow® BSP provides control of all the 3316's hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek's GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3316 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973 IP with their own.

Model 3316 Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC

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