

Model 2266B

Features

Best Source Selector

- Up to 16 channels per chassis
- Works with encrypted data
- Input stream correlated in time
- Seamless stream switching on bit boundaries (down stream frame syncs do not drop lock).
- Multiple Selection Criteria
 - Measured Long-Term Signal Quality
 - Measured Short-Term Signal Quality
 - Sync Pattern Detection
 - Convolutional Lock
 - Bit Sync Lock and Signal Present
 - Bit-by-bit Majority Vote Weighted by Signal Quality
 - Short Term Bit-by-bit Quality
 - Error Correction
 - 3.3 dB Typical Link Performance Improvement
- Encapsulated Data Input (Option)
- Receives Data and Quality from upstream unit (MD265E)

Multi-Channel Bit Synchronizer

- Up to 16 Channels
- Bit Rates
 - 5 bps to 20 Mbps (40Mbps Opt)
- Hot Swap Redundant Power Supplies
- Performance within 1 dB of theory
- Loop Bandwidth Settings from 0.01% to 1.6%
- Accepts NRZ-L/M/S, BiØ-L/M/S, DM-M/S; MDM-M/S
- Randomizer/Derandomizer
- Scrambler/Descrambler
 - CCITT V.35/36
- Viterbi Decoder
- Frame Pattern Detector
- Advanced Lock Detection
- QPSK/OQPSK/SOQPSK Resequencer (Optional)
- Remote Control via
 - RS-232 (Std)
 - IEEE-488, Enet (Optional)
- 7-inch High Chassis

General Description

The GDP Model 2266B Multi-Channel PCM Bit Synchronizer/ Best Source Selector houses up to sixteen high-performance bit synchronizer modules. Each individual channel can be used



as a normal Bit Sync and/or selected as a source for Best Source Selection. The optimized digital design of this unit affords the highest performance characteristics currently available. The unit operates to 40Mbps (20Mbps Standard, 40Mbps optional).

The standard IRIG randomizer/derandomizer for both forward and reverse sequences is provided. CCITT V.35 and V.36 scrambling/descrambling is also provided. A variety of Viterbi decoders are available including R1/2 K7, R3/4 K7 and R1/3 k7 (please inquire for other FEC options).

The unit can also be provided with an optional QPSK resequencing function that supports QPSK, OQPSK and SOQPSK data streams.

Best Source Selection of Non-Encrypted and Encrypted Data based on Signal Quality

The GDP Space Best Source Selector is an advanced, next generation implementation of best source selection based on signal/ data quality. Since signal quality is used in the decision making process, the unit does not need to see the synchronization pattern and the data can be encrypted. A digital data mode is also available for the case where receivers are located remotely and the analog signal is not available.

The unit can be divided into three major sections, Bit Synchronizer, Path Alignment, Path Selection. The Bit Synchronizers are providing data, clock, short-term data quality (signal quality of a small group of bits) and long-term data quality (signal quality over several hundred bits) to the Path Alignment and Path Selection sections. The Path Alignment section consists of correlators and path delay/advancement correction (works on encrypted streams). The Path Alignment section provides data, aligned in time, to the Path Selection.

The Path Selection section uses the short-term and long-term data quality in addition to lock status to determine the best path. The unit provides the capability to switch data streams based these quality measurements. Depending upon the number of valid sources, bitby-bit output values are selected. This is accomplished by a Majority Voting technique weighted by signal quality. This automatic mode provides error correction that results in better then a 3.3dB performance improvement of the link.



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Best Source Selector—General

Current Best Source Selection (BSS) techniques rely on two processes for selecting the source of the best available signal for further processing. The primary method of detecting the best signal is by detecting the frame synchronization pattern contained in the PCM formatted stream. The second process requires prior knowledge of the path of the aircraft or missile so that the source can be changed on a priority basis as it deteriorates at the current source. The use of this method allows the danger of losing significant amounts of data before a source switch can be made. Of even greater importance, the frame sync pattern recognition technique cannot be used if the entire data stream is encrypted, without first decrypting all of the data.

GDP Space Systems has studied the process of selecting the best signal source and is offering an alternative method that addresses the issues presented above. Probably, the most serious problem is the problem of data loss due to switching process and/or noise bursts. These error bursts typically happen at the worst possible time, when the maneuver is being performed. The second issue is the issue of dealing with encrypted data. This issue is becoming quite important as encryption becomes more prevalent in the test community.

This document presents a new, next generation of best source selection techniques that can overcome both of these difficulties. This new approach looks at the raw received baseband signal itself along with the data and uses signal quality measurements to determine the best output on a bit-by-bit basis. A significant performance gain (several dB) can be achieved through these advanced data correlation and error correction techniques.

The technique used to select a best source of received telemetry data is based primarily on finding the data source with the best measured long-term signal quality. Using a proprietary technique, a method of measuring signal quality is accomplished in the Bit Synchronizers that is quite accurate once the synchronizer acquires Lock. The signal quality measurement can be used for any type of input data including data that has been encrypted. Both long-term signal quality (taken over a large number of bits) and short term signal quality (taken over a small group of bits) measurements are taken. The signal quality measurement is unaffected by the data content other than the transition density. The fact that the data is encrypted actually helps in that the process generally improves the transition density in the same way that randomizing is used to improve transition density.

Another function of the best source selection process is the ability to switch sources without causing the down stream Frame Synchronizer connected to the Bit Synchronizer/Best Source Selector output to lose lock. This allows the user to continue processing the stream after a source switch, without loss of data. The recovered clocks of the input data must be corrected to match the phase of the recovered clock of the currently selected output. This is accomplished by the addition of phase delay in the newly selected bit sync recovered clock until it closely matches the phase of the currently selected bit synchronizer. The next process aligns the data in each valid source. Data from the currently selected source is delayed through a programmable length delay device. The programmed delay length is based on the maximum possible path delay between any of the input sources and is useful in keeping the system latency to a minimum. Only after the data is aligned will the source switch take place. This process can also be used with encrypted data since no fixed pattern is used to correlate the sources. A Sequential Probability Ratio test is used to correlate the data from the sources. This means that the data does not have to be completely error free in order to be correlated. Once correlated, several techniques are used to correct the data depending on how many valid sources are available.

The unit uses long-term and short-term signal quality to determine the best output at any point in time on a bit-by-bit basis. An automatic "Majority Vote" mode is also supported by the unit. This mode varies depending on the number of streams available. With two valid data sources the long-term and short-term (bit-by-bit), data quality is used for the determination of the particular output bit location. If three or more sources are available, then Majority Vote technique (weighted by signal quality) is used. Since these methods perform error correction, both two source and three or more source situations provide a significant performance gain (better then 3.3dB typical).



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Best Source Selector-General con't.

By using this processes, the selection of the best source of the same data from multiple sources can reliably be identified and a transparent switch from one source to another can be accomplished without the loss of data.

In some situations the receivers are located in a remote area, and the digital signal is sent to a central location where Best Source Selection occurs. For this configuration the MD2266B BSS unit can be used in conjunction with the GDP MD2265E or MD2266E Bit Synchronizer/BSS Encapsulation units. The MD2265E is located at the remote site and will act as a local bit synchronizer. It will also encapsulate the date (encrypted or clear) along with the signal quality information into a transfer frame. The digital data stream is then transmitted to the central MD2266B BSS unit where the data and quality information is extracted and used by the BSS algorithm. In this situation the BSS achieves the full performance gain previously defined for both two stream missions and missions with three or more streams. The BSS located in the central location can be programmed to process a mix of local and remote (encapsulated) streams.

If the remote site already has bit synchronizers the digital data can be sent to the MD2266B BSS at the central location without the signal quality information. In this mode the digital data (encrypted or clear) from the legacy remote bit synchronizers is routed to the MD2266B BSS at the central location. This is typically done through multiplexers, microwave links and fiber. Data switching at the central MD2266B BSS will occur based on data quality. A significant performance gain is also achieved in this configuration but error correction can not be achieved without 3 or more sources.

Best Source Selector—Overview

The GDP Model 2266B Multi-Channel PCM Bit Synchronizer/Best Source Selector houses up to sixteen high-performance bit synchronizer input modules, up to eight Best Source Selector (BSS) output modules, a control processor and redundant power supplies (optional). Each individual channel can be used as a normal Bit Synchronizer and/or selected as a source for Best Source Selection. Each Bit Synchronizer input module is an independent channel designed to extract usable digital data from a noise contaminated signal environment.

Bit synchronizer modules measure the long-term signal quality and a short-term signal quality from which the real-time error rate (data quality) of the live data stream can be determined. The process of selecting the best source of data is based on programmed criteria. Any or all of these criteria can be used in the BSS decision process. Programmable criteria are:

- 1. Measured Long-Term Signal Quality
- 2. Measured Short-Term Signal Quality
- 3. Sync Pattern Detection
- 4. Convolutional Decoder Lock
- 5. Bit Sync Lock and Signal Present

The GDP Best Source Selector can be divided into three major sections, Bit Synchronizer, Path Alignment, Path Selection. The Bit Synchronizers are providing data, clock, short-term data quality (signal quality of a small group of bits) and long-term data quality (signal quality over several hundred bits) to the Path Alignment and Path Selection sections. The Path Alignment section consists of correlators and path delay/ advancement correction. The Path Alignment section provides aligned data paths to the Path Selection section uses the short-term and long-term data quality in addition to lock status to determine the best path. With 2 or more sources, bit-by-bit values are selected for output.



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Best Source Selector—Overview con't.

Current Best Source Selectors that correlate all possible data paths, based on the frame sync pattern, require a decryption device per data path, this becomes a costly solution. The GDP Space Best Source Selector uses a long-term signal quality measurement and other sync criteria to correlate the data paths. The Path Alignment section that has the correlators does not require a frame sync pattern. These correlators are periodically programmed with the estimated best path data, which allows the correlators to handle both encrypted and non-encrypted data.

Correlating the data paths is only half the Best Source solution; the other function is making a decision on the best path or the best current bit. The GDP BSS uses two techniques for determining the best path. The first is the long-term signal quality. Based on this measurement, streams are switched on bit boundaries, always allowing the best stream to be output at any point in time. This is based on a programmed difference in performance (i.e. "N" dB better). The second mode of operation is the Majority Vote mode. In this mode the short-term signal quality measurement is used along with the long-term signal quality to provide a bit-by-bit reconstructed output stream. This mode provides a significant link performance increase of better then 3.3 dB (typical), and is discussed in further detail later in this document.

The external signal interfaces for each Bit Synchronizer and BSS Interface modules (IFB's) are at the rear of the Model 2266B. Two types of IFB modules are used (Refer to Figure 1 Below). The first is the IFB607-1. This module supports Best Source Selection. Up to eight IFB607-1 (Best Source Selection) IFB modules can be used in the case where four BSS groups are required. A single BSS IFB module will allow selection of up to sixteen (best of 16). Two BSS IFB's will allow 2 groups of best of 8, Four BSS IFB's will allow selection of 4 groups of best of 4 and so on. The second type of IFB modules (IFB607-2), are plugged into the remaining rear slots that do not contain the IFB607-1 boards. These modules allow I/O from individual bit synchronizers. Bit Synchronizers not being used as Best Source Selector channels can be used as individual bit synchronizers.

The CPU011 Control Processor provides the control path between the operator interfaces (front panel or remote control interface port), the BSM602 (Bit Synchronizers) and the IFB607 (Best Source Selector Interface Cards). The CPU011 is and embedded processor with PROM based firmware and is not hampered by a cumbersome non-deterministic operating systems like XP, Windows 2000 or NT. Operating parameters for each Bit Synchronizer are selected using an interactive menu on the front panel for formatted commands from the remote user control port. The Remote Control port is an RS232 serial interface. IEEE-488 and Ethernet remote control interfaces can be provided as an option.



Figure 1 Eight Channel BSS Rear View



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Majority Vote Weighted by Signal Quality Performance Increase of Better Than 3.3dB

In the Majority Vote mode both a bit-by-bit voting and signal quality information are used in the determination of the correct output bit (Refer to Figure 2). The long-term signal quality is very accurately measured over several hundred bits. This is used in the validation of possible candidate streams. For short-term signal quality a sliding window is used across small group of bits. The BSS then looks at 'N' number of bits before and after the bit in question and provides a bit-by-bit quality output stored along with the data for each of the candidate streams. To achieve the full benefit of the Majority Vote mode, you need three or more streams. However, a significant performance gain is still achieved with only two streams. With this mode enabled, when you have only two valid streams they are automatically correlated in time. The bit-by-bit output is then determined on the bit-by-bit signal quality. For example: If one of the two streams has a signal quality which is 5dB better then the other stream the bit value of the better stream will be output in that bit location. Although error correction occurs in this mode, maximum error correction performance is achieved when three or more valid sources are present.

When a 3^{rd} source comes on-line it is automatically correlated with the other two sources, and full majority voting (weighted by the short and long term Quality) is invoked. For example: With 3 sources, the corresponding bit location in each of the sources will be examined and a vote will occur with the signal quality bits present to determine the validity of the data bits. This mode corrects the output data stream when error bursts occur due receiver fades and/or multi-path. A substantial link performance gain is achieved in this mode of better then three times the error rate squared (i.e. three sources with an error rate of 10^{-6} result in an output error rate better then 3×10^{-12}). Also see the following performance graph.



Figure 2 Model 2266B Multi-Channel Bit Sync / Best Source Selector Majority Vote Mode (Weighted by Signal Quality)



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Figure 3 Best Source Selector Performance Gain

A	Bit Error Rate for Single Source with Rayleigh Distributed SNR	D	Perfect 3 Source BSS (assumes we are always able to pick the best source).
B	Perfect 2 Source BSS (assumes we are always able to pick the best source).	Ε	Modified Majority Vote of 3 Sources us- ing signal quality.
С	Pure Majority Vote of 3 Sources not using signal quality.		



Signal Inputs

MULTI-CHANNEL PCM BIT SYNCHRONIZER AND BEST SOURCE SELECTOR

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SPECIFICATIONS

Signal Inputs	
Inputs per Channel (8 Ch. Max.)	Three (3) Analog or Digital [Other I/O configurations Available]
Input Impedance	Lo Z: 50 ohms (optional 75 ohm) or High Z (Selectable)
Levels	0.25 Vp-p to +/- 12 Vp-p or RS-422 (Optional)
DC Offset	100% of the input peak-to-peak signal level.
AC Offset	No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Input Codes	NRZ-L/M/S, BIÓ-L/M/S, DM-M/S, MDM-M/S
De-randomizer	RNRZ De-randomizer fwd and rev per IRIG-106
Polarity	Normal / Inverted.
Viterbi Decoder	*Constraint length 7, rate $\frac{1}{2}$, G1 =171 octal G2= 133 octal G1/G2 Swap and G2 Invert (other viterbi options available)
	*Differential Decoder and Descrambler (V.35 & V.36)
Eb/No Measurement	-2 to $+20$ dB 0.5 dB resolution
Synchronization	
Bit Rate Range	40 bps to 20 Mbps (40Mbps optional)
Tuning Resolution of Bit Rate	$X.XXXE^{N}$ (1 \leq N \leq 7)
Capture Range	Equal to LBW
Loop Bandwidths	0.01% to 1.6%
Sync Threshold	SNR –3 dB for NRZ, (-1 dB for BIÓ) codes, square-sided data.
Sync Maintenance	SNR –3 dB with transition density 50%, LBW1 w/ NRZ-L
Sync Acquisition	50 bits or less
Sync Retention	256 bits without transitions, LBW1.
Bit Error Rate	Within 1 dB of theory over the full bit rate range
Frame Pattern Detector	Detection of up to 32 bits

Outputs, each Bit Sync Channel

TTL (Each Channel)- Two Coded PCM and Two Clocks (Programmable 0, 90, 180, 270 degrees), plus one Selected Data & Clock Output for BSS Channels

RS422 (Each Channel)- Two Coded PCM and Two Clock (Programmable 0, 90, 180, 270 degrees), plus one Selected Data & Clock Output for BSS Channels

Bipolar Tape Output (Each Channel)- One +/-1V - Coded PCM

Lock Status - Bit Synchronization, Frame Pattern and Viterbi

Signal Quality Status: Eb/No, Deviation, Frame Sync Pattern Error Count, Viterbi Error Count and BERT / PRN BER Measurements on Front Panel Display and Remote Port

Ordering Information

MD2266B-XX Basic Unit (20Mbps) includes 1 BSS Group
Majority Vote also included in Base MD2266BOP2266B-10IEEE-488 Remote Control
OP2266B-21-XX = -04, -06, -08, -10, -12, -14 or -16 ChannelsOP2266B-21Ethernet Remote ControlOP2266B-01Extended Bit Rate 5 bps to 40 MbpsOP2266B-40Additional BSS Groups (up to 7 additional)OP2266B-05QPSK & OQPSK OptionOP2266B-41Special I/O Transition ModuleOP2266B-06SOQPSK OptionOP2266B-50Redundant Power SupplyOP2266B-07QPSK & OQPSK & SOQPSKOP2266B-89Rack Mount Shelf Kit

Recognizing that no standard product can meet all the needs of all		The statements in this data sheet are not intended to create any war-
users, GDP stands ready to provide units tailored to unique		ranty, expressed or implied. Equipment specifications are subject to
applications.		change without notice.

URL: http://www.gdpspace.com E-mail: gdpinfo@gdpspace.com

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