MULTI-CHANNEL PCM BIT SYNCHRONIZER

Model 2266

Features

- Up to 8 Channels
  Up to 16 Channels (Opt)
- Bit Rates
  - 5 bps to 20 Mbps
  - 5 bps to 40 Mbps (Opt)
- Hot Swap Redundant Power Supply
- Performance within 1 dB of theory
- Loop Bandwidth Settings from 0.01% to 1.6%
- Accepts NRZ-L/M/S, BiØ-L/ M/S, DM-M/S; MDM-M/S
- Status Indicators
  - Sync and Loss
- Bit Rate Deviation Display
- Randomizer/Derandomizer
- Scrambler/Descrambler
  CCITT V.35/36:
- Viterbi Decoder
- Frame Pattern Detector
- Signal Quality Status
  - Eb/No Measurement
  - Frame Sync Pattern Error Count (BER Status)
  - Viterbi Error Count
  - BERT/ PRN BER Measurement
- Advanced Lock Detection
- Auto Bit-Rate Scan (Opt)
- QPSK/OQPSK/SOQPSK Resequencer (opt)
- Remote Control via.
  - RS-232 (Std)
  - IEEE-488, Enet (Opt)
- 7-inch High Chassis

General Description

The GDP Model 2266 Multi-Channel PCM Bit Synchronizer houses up to eight high-performance bit synchronizer modules. The optimized digital design of this unit affords the highest performance characteristics currently available.

The Model 2266 is capable of maintaining synchronization with the signal of interest down to –3 dB Eb/No. When searching for the signal, acquisition is attainable in less than 50 bits. The unit is very robust and can maintain synchronization for a period of at least 256 bit periods without a transition.

The standard IRIG randomizer/derandomizer for both forward and reverse sequences is provided. CCITT V.35 and V.36 scrambling/descrambling is also provided. A variety of Viterbi decoders are available including R1/2 K7 (Std), R3/4 K7 and R1/3 k7 (please inquire for other FEC options).

The MD2265 includes several unique features to determine the quality of the data. The first is an Eb/No (Signal Quality) measurement. From this measurement the error rate of the data can be determined. The BSM201B also measured errors in the frame synchronizer pattern as well as errors in the viterbi stream when these modes are enabled. A bit-error-rate (BERT) function is also provided. This allows link test in a short loop-back to verify proper operation of the module, or long loop-back to measure performance of the link. An advances lock detector ensures a solid lock indication for the module.

To assure synchronization to the intended data stream, the Frame Pattern Detector may be invoked. Up to a 64-bit long pattern is detected. Maintaining synchronization with this pattern at the programmed repetition rate and synchronization strategy produces a lock signal. An Automatic Polarity Correction (APC) mode is also provided for inverted data.

The optional Auto Scan feature is available to scan the input for up to 8 combinations of bit rates, input codes and frame patterns (per Bit Sync channel). When one of the signals is present the Bit Sync automatically locks onto it and recovers the data and clock.

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SPECIFICATIONS

Inputs, each Bit Sync

Analog Inputs	Up to 4 Inputs per Bit Sync- 50 ohms (optional 75) or High Z (Transition Module Dependent)
Digital Inputs	Differential RS-422 and TTL (Optional)

Performance

Bit Rate Range	5bps to 20 Mbps (40 Mbps Optional)
Tuning Resolution	$X.XXXE^N$ ($1 \leq N \leq 7$)
Input Levels	0.2 Vpp Min., +/- 12 V Max.. (others available)
DC Offsets	100% of the input peak-to-peak signal level.
AC Offset	No degradation up to 100% of input signal amplitude at 0.1% of the bit rate.
Loop Bandwidths	0.01% to 1.6%
Acquisition Range	2x LBW
Sync Acquisition Threshold	SNR 0 dB
Sync Maintenance	SNR –3dB
Sync Acquisition	< 50 bits
Sync Retention	256 bits without transitions
Bit Error Rate	1 dB to 40 Mbps

Features

Input/Output PCM Codes	NRZ-L/M/S, BIØ-L/M/S, DBIØ-M/S, DM-M/S; MDM-M/S
Randomizer/Derandomizer	IRIG 106-96 forward and reverse
Descrambler	CCITT V.35/V.36
Viterbi Decoder	R 1/2, K 7 with G1/G2 Swap and G2 Invert, (others available)
Resequencer	QPSK/OQPSK/SOQPSK (Optional)
Frame Pattern Detector	Up to 64 bits with programmable strategy and APC
Auto Scan (Optional)	Searches up to 8 Bit Rate, Code, Frame pattern combos per Bit Sync
Output Data Polarity	Input polarity normal / inverted.
Output Clock Phase	0, 90, 180, 270 degrees

Outputs, each Bit Sync Channel

TTL (Each Channel)- Four Coded PCM and Three Clocks (Programmable 0, 90, 180, 270 degrees)
RS422 (Each Channel)- Two Coded PCM and Two Clock (Programmable 0, 90, 180, 270 degrees)
Bipolar Tape Output (Each Channel)- One +/-1V - Coded PCM
Front Panel Monitor (Each Channel)- One Selected Input Monitor, one PCM Data Out, one Clock Out
LOCK STATUS - Bit Synchronization, Frame Pattern and Viterbi
Signal Quality Status: Eb/No, Deviation, Frame Sync Pattern Error Count, Viterbi Error Count and BERT / PRN BER Measurements on Front Panel Display and Remote Port

Ordering Information

R261211

MD2266-XX	Basic Unit (20 Mbps)
MD2266-04	FOUR CHANNELS
MD2266-06	SIX CHANNELS
MD2266-08	EIGHT CHANNELS
OP2266-01	Operation to 40 Mbps
OP2266-05	QPSK & OQPSK Resequencer
OP2266-06	SOQPSK Resequence
OP2266-10	IEEE-488 Remote Control
OP2266-21	Ethernet Remote Control
OP2266-43	BERT Option
OP2266-45	Auto Bit-Rate Scan Option
OP2266-50	Redundant Power Supply Option
OP2266-90	Recirculate (NRZ-L & Clk In/ RNRZ Out)

Recognizing that no standard product can meet all the needs of all users, GDP stands ready to provide units tailored to unique applications.

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