GDP SPACE SYSTEMS

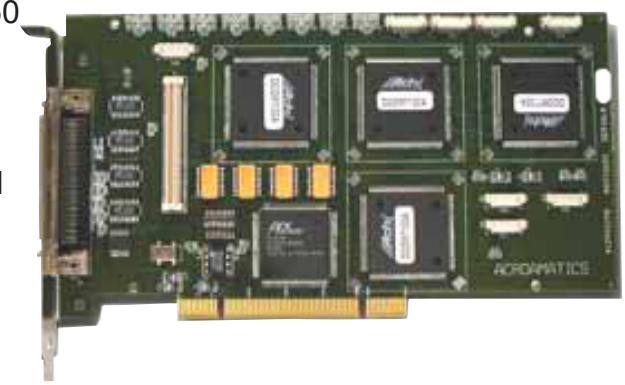
ACROAMATICS
TELEMETRY SYSTEMS

Frame Sync Verification Unit
Model 1650P

Features:

- 8 - 32 Mbps
- Eight Channel
- Automatic Polarity Inversion
- Optional: Time Code Translator Generator

General Description



The Model PCI 1650 FSVU (Frame Synchronization Verification Unit) contains eight PCM Decommutators that are designed for PCM stream quality verification rather than data processing. Each decommutator contains a minor frame synchronizer with a 64 bit pattern correlator, a 16 bit counter that counts the number of bits per frame and a programmable synchronizer strategy providing Search, Verify and Lock states. A programmable watchdog timer returns decommutation to Search if the input clock is lost. The status of each of the eight decommutators can be read over the PCI bus to determine the quality of the input data to each channel.

The Model 1650P is an integrated component of the Acroamatics Model 2602 Best Source Selector. The Model 1650's GUI controls system setup, file storage and recall, system configuration/monitoring, status generation and self-tests.

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Signal Inputs

Source	Eight channels, each accepting RS-422 differential 0° clock & NRZ data
Impedance	120Ω input impedance, TTL compatible
Bit Rate	Up to 20 Megabits per second
Polarity	Programmable, with automatic polarity correction
Frame Length	Programmable, 16 to 16384 bits

Synchronization

Mainframe Sync	Provides for programmable sync pattern and mask, complement pattern recognition, and variable length frame decommutation. Pattern length up to 64 bits.
Alternate Complement Sync	Synchronizes to formats in which the minor frame sync pattern is complemented on alternate frames
Complement Frame Sync	Synchronizes to formats that complement the minor frame sync pattern at a major frame rate
Automatic Polarity Inversion	Input polarity is inverted when two consecutive complemented sync patterns are found.
Sync Modes	Fixed, Adaptive and Burst
Sync Strategy	Search, Verify and Lock
Sync Error Tolerance	0 to 15 errors, programmable
Sync Slip Window	0, ±1, ±2 & ±3 bits, programmable
Data Polarity	Normal, Inverted and Automatic detection
Clock Rate Monitor	A programmable delay counter is provided to return the synchronizer to Search if the clock input is lost.

Output

Time	The Time Code Translator can be read from the PCI bus.
PCM Status	A status word is available for each PCM frame synchronizer via the PCI bus.
Discrete Status	The Lock status of each frame synchronizer is output as an RS-422 signal
Serial Setup Output	A serial RS-422 output allows you to send data from the PCM bus to an external device.
CVT	128k x 32 bit CVT memory, addressed by assigned PCM word ID tag. Read by the PCI bus, it contains last value from up to 128k TM sources.
Block Buffer Memory	Used to format and input up to 512k messages of 32 bits words. Six programmable formats: 4 with ID tags and 2 data only. May include programmable time stamp and header message.
DMA	Dual buffered DMA channel for transferring messages formatted for the block buffer memory directly to Host memory.
Mezzanine Card	A mezzanine connector supports an optional Time Code Translator/Generator (with or without PCM/PAM Simulator). The mezzanine card provides the following signals: IRIG B In Amplitude modulated IRIG A. B or G with 100mV to 10V peak to peak signal input amplitude. Simulator output is RS-422 NRZ-L data and 0° clock.

Physical

Format	Standard PCI: half length single slot
Cooling Requirements	30 Linear FPM
Power Requirements	+5VDC at 1A, +3.3VDC at 2A
Dimensions	4.20” (10.67cm) H x 7.6” (19.15cm) W x 0.55” (1.4cm) D
Temperature	Operating 0° to +40° C, Non-Operating -40° to +86° C
Relative Humidity	Up to 90%, non-condensing
Shock	Operating 6G, Non-Operating 25G
Vibration	Operating 0.3G, 5 to 2000 Hz, Non-Operating 0.8G, 5 to 500 Hz

Specifications subject to change without notice.

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