



High-Speed Switched Serial Fabrics Improve System Design

Sixth Edition

Switched Serial Fabrics

FPGA Resources

Products

Applications

Links

by

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Preface

As evolutionary enhancements to the venerable VMEbus, both VXS and VPX deliver significant improvements in data bandwidth, connectivity, power distribution, and cooling. When VME was first introduced, its shared bus backplane interboard transfer rates of 30 or 40 MBytes/sec were more than adequate for most applications. As requirements grew, VME acquired new interfaces such as VSB, RACEway, RACE++, VME64, VME320, and 2eSST, thereby ensuring a healthy community of suppliers and a new stream of products.

Well into its third decade of widespread deployment, VME adopted the new VXS gigabit serial interface, clearly representing the most significant leap in backplane data transfer rates throughout its entire history.

Because VXS delivered such a dramatic improvement in embedded system performance, the use of gigabit serial technology was extended to create VPX. The OpenVPX initiative followed shortly thereafter, as risk-averse government agencies mandated the need for industry-wide standards. The hallmark of any successful standard is that it continues to evolve with technology, and none offers a better example than VME's evolution to VXS and VPX.

In a similar venue, the PMC mezzanine card, became the dominant architecture for mezzanine I/O in VMEbus-based embedded systems. PMC was successfully adopted for both commercial and government electronic systems. In the following years, important extensions to the PMC standard included ruggedized and conduction-cooled versions for severe environments and the adoption of the processor PMC specification. With the adaption of gigabit serial interfaces, XMC, a natural extension of that technology to PMC modules, followed soon.

For more information on complementary subjects, the reader is referred to these other Pentek Handbooks:

Critical Techniques for High-Speed A/D Converters in Real-Time Systems

Software Defined Radio

Putting FPGAs to Work in Software Radio Systems

High-Speed, Real-Time Recording Systems

Switched Serial Fabrics

Switched Serial Gigabit Interfaces - Why?

- Too many different I/O technologies per system
 - FPDP, PCI, VME, Ethernet, RS-232, FibreChannel, SCSI, PMC, IP, 1553, LVDS, ATM, etc.
- Bus backplanes are major data bottlenecks
 - All boards must share a common bus, one at a time!
- Parallel switched fabrics are expensive
 - RACEway was controlled by one vendor
- Cabling increases system cost and complicates maintenance
 - Cables and connectors can be a major factor in MTBF
- Software upgrades are difficult for specialized interfaces
 - Performance goals require software tuning of signal paths
- Need a better solution for moving data !
 - Fast, flexible, open, and inexpensive



Figure 1

The VMEbus still serves as the dominant bus structure for high-performance real-time embedded systems. As requirements grew following its introduction, VME acquired new interfaces such as VSB, RACEway, RACE++, VME64 et al. that provided improved performance.

All these different I/O technologies caused new problems with backplanes creating data bottlenecks and interfaces controlled by one vendor. System costs increased due to cabling, maintenance and software upgrades. A better solution for moving data was needed and it had to be fast, flexible, and inexpensive.

The answer turned out to be Switched Serial Gigabit Interfaces.

High-Speed Switched Serial Interfaces

- Gigabit serial links send data over a pair of wires using differential signaling
- Sequential 1s and 0s are sent over the pair of wires at a fixed bit rate
 - Popular serial rates: 10 MHz, 100 MHz, 1 GHz, 2.5 GHz, 3.125 GHz, etc.
- The clock, data, and data word framing are encoded into the serial bits stream, typically using 8B10B coding:
 - 10 bits of serial transmission are required to deliver 8 bits of data
 - Extra 2 bits maintain synchronization, framing and DC line balance
- SERDES - Serializer / Deserializer
 - Serializer: Encodes clock, frame, and 8 bits of data into a 10-bit stream
 - Deserializer: Decodes clock, frame and 8 bits of data from a 10-bit stream
 - Usually combined into one device for full duplex operation

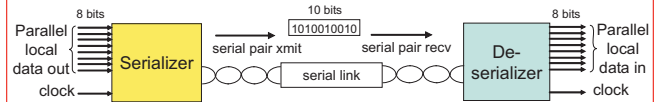


Figure 2

A switched serial fabric system connects devices together to support multiple simultaneous data transfers, usually implemented with a crossbar switch. Using differential signaling, data is sent over a pair of wires at a fixed bit rate such as 100 MHz, 1 GHz, 2.5 GHz, 3.125 GHz, etc.

The clock, data, and data word framing are encoded into the serial stream, usually with 8B10B coding. Ten bits of serial transmission deliver eight bits of data. The extra two bits maintain synchronization, framing and DC line balance.

The Serializer shown in Figure 2 encodes clock, frame, and eight bits of data into a 10-bit stream. The Deserializer decodes the 10-bit stream into clock, frame, and eight bits of data. These two functions are usually combined into one device for full duplex operation, known as the SERDES (SERializer/DESerializer).

Switched Serial Fabrics

Gigabit Serial Data Rates

- Gigabit Serial Data Transfer Rates Depend On:
 - Serial clock frequency (serial bit rate)
 - Number of bit “lanes” ganged together (e.g., 4X = 4 bit lanes)
 - Physical layer encoding overhead (8B10B): 80% Efficiency
 - Peak Rate (MB/sec) = (Serial Rate x Lanes x 80%) ÷ (8 bits per byte)

$$= (\text{Serial Rate} \times \text{Lanes}) \div 10$$

Peak Rates for Specified Number of Bit Lanes				
Bit Clock	1X	4X	8X	16X
1 GHz	100 MB/sec	400 MB/sec	800 MB/sec	1.6 GB/sec
2.5 GHz	250 MB/sec	1.0 GB/sec	2.0 GB/sec	4.0 GB/sec
3.125 GHz	312 MB/sec	1.25 GB/sec	2.5 GB/sec	5.0 GB/sec
5.0 GHz	500 MB/sec	2.0 GB/sec	4.0 GB/sec	8.0 GB/sec
10.0 GHz	1.0 GHz/sec	4.0 GHz/sec	8.0 GB/sec	16.0 GB/sec

Figure 3

The raw speed of serial fabrics is governed by three factors:

The serial bit clock frequency; the inherent 8B10B channel encoding efficiency of 80%; and the number of lanes or parallel bit streams ganged together in the interface.

Since there are 8 bits per Byte, the peak rate expressed in MB/sec becomes the serial rate expressed in GHz, times the number of lanes, divided by 10.

For example, VXS with four bit lanes or 4X, the peak transfer rate in each direction is the serial bit clock divided by 2.5.

The table above shows the transfer rates for each VXS link for 1, 2.5, 3.125, 5.0, and 10 GHz bit clocks.

Of course, there is some additional overhead in the packet protocols, some of which are presented next.

Popular Gigabit Serial Protocols

Popular Gigabit Serial Protocols

- Xilinx Aurora
 - Low-level Link-layer protocol, with optional framing
 - Point-to-point links, primarily for raw data
 - Interfaces on Virtex-II Pro, Virtex-4 and Virtex-5 FPGAs
- VITA 49 – Digital IF Protocol (VRT)
 - Built on top of Aurora link layer protocol
 - Point-to-point links, primarily for digitized IF signals
 - Packet headers include signal descriptors
- PCI Express
 - Memory-Mapped Fabric
 - Personal computer connectivity, replacing PCI bus
 - Board-to-board and peripheral support
- Serial RapidIO
 - Packet Switched Fabric
 - Targeted for COTS and embedded multi-computing
 - Chip-to-chip, board-to-board, and peer-to-peer



Figure 4

Xilinx offers a simple link layer protocol IP core engine called Aurora that interfaces with the RocketIO gigabit serial physical layer interfaces available in the Virtex-II Pro family.

Altera supports its Stratix GX Multi-Gigabit Transceivers with the SerialLite link layer protocol as well as full implementations of switched fabric IP cores.

The nice thing about this strategy is that you can design and build FPGA-based hardware products that adapt to different fabrics, depending on the protocol IP core you install.

VITA 49 is a radio transport protocol for SDR (Software Defined Radio) architectures that enables interoperability between diverse SDR components from different vendors

PCI Express is Intel’s initiative for connectivity between processors and boards in personal computers and workstations. It’s been used extensively to improve performance of graphics boards in Windows computers.

RapidIO is a packet-switched fabric targeted for embedded computer component vendors and system integrators. It addresses the needs of real-time computing at several levels.

Switched Serial Fabrics

Dedicated Point-to-Point Serial Links

- Dedicated Hardwired Connections
 - Paths are based on particular application requirements
 - Paths set up during system integration with cables or fixed wiring
 - Applications: Aurora, VITA 49, PCI Express, Serial RapidIO

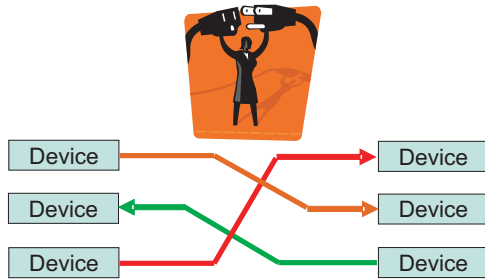


Figure 5

The first type of serial links is the dedicated point-to-point link. As its name implies, it utilizes dedicated hardware connections and its paths are based on the requirements of the particular application. The paths are set up during system integration and utilize cables or fixed wiring.

Applications that utilize dedicated point-to-point serial links include those that are running Aurora, VITA 49, PCI Express and RapidIO.

Manually-Switched Point-to-Point Links

- Software Configurable “Protocol Transparent” Switch
 - Switch paths are changed in hardware “manually” by a control processor
 - Paths can be changed during initialization and during runtime
 - Switch is transparent to the serial protocol
 - Switch supports virtually all gigabit serial links
 - Applications: Aurora, VITA 49, PCI Express, Serial RapidIO
 - Switching Scheme for Pentek 4207

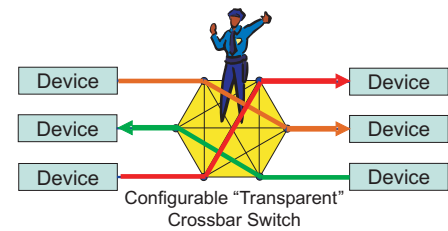


Figure 6

Next in line are manually-switched point-to-point serial links. Think of them as “protocol transparent” switches that are software configurable. In this case the switch paths are changed in the hardware “manually” by a control processor that directs the traffic. They can be changed during system initialization and during runtime.

This switch supports virtually all gigabit serial links and it’s transparent to the serial protocol. It can be used in applications running Aurora, VITA 49, PCI Express and Serial Rapid IO.

This type of switch is used in the Pentek Model 4207 PowerPC I/O Processor. More about this VME/VXS board in the Products and Applications sections.

Switched Serial Fabrics

Memory-Mapped Serial Links

- One system processor establishes memory map for all devices
 - This function is known as the “root complex”
- Switches or bridges implement defined memory mapped connections
- Supports multiple “initiators” and multiple “targets”
- Arbitration is done through token passing
- Does not provide automatic re-routing
- Example: PCI Express

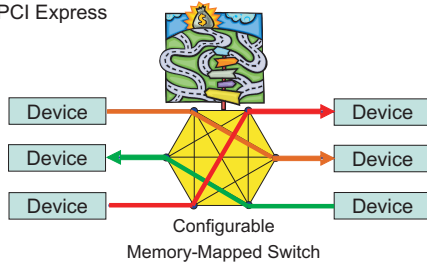


Figure 7

Memory-mapped serial links are based on a memory map that's established by a system processor.

The defined memory-mapped connections are implemented with hardware switches or bridges.

This type of link supports multiple “initiators” and multiple “targets”. Arbitration is done through token passing and automatic-rerouting is not supported.

A protocol example that uses this link is PCI Express.

Packet-Switched Serial Links

- Switched “fabric” protocol uses data packets that include:
 - Header information to identify source, destination, packet type, data size, time stamp, sequence number, and priority
 - Data “payload”
 - Footer information for checksum and end of packet marker
- Intelligent switch evaluates packet header to determine routing
- Automatic re-routing through alternate switch paths avoid conflicts
- Packets and Switch are unique and dedicated to a particular protocol
- Supports multiple processors
- Example: Serial RapidIO

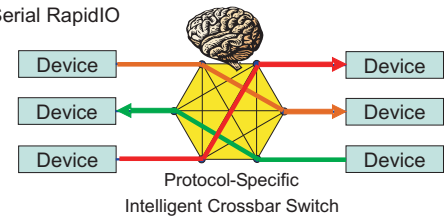


Figure 8

Packet-switched serial links utilize a switched fabric protocol that uses data packets. Each data packet includes:


- A header that provides information to identify the source, destination, packet type, data size, time stamp, sequence number and priority
- The data “payload” which contains the actual data
- A footer with checksum and end of packet marker information

This intelligent switch evaluates packet header information to determine the routing. Automatic rerouting through alternate paths avoids conflicts. The packets and the switch support multiple processors. They are unique and dedicated to a particular protocol

Applications running Serial RapidIO can utilize this packet-switched fabric.

Switched Serial Fabrics

Comparison of Serial Links



	Dedicated Point-to-Point	Manually Switched Point-to-Point	Memory Mapped Fabric	Packet Switched Fabric
Software Reconfigurable Paths	No	Yes	Yes	Yes
Self-Routing Packets	No	No	No	Yes
Automatic Path Re-Routing	No	No	No	Yes
Packet Overhead Required	Low	Low	Med	High
Payload Data Efficiency	High	High	Med	Low
Software Driver Complexity	Low	Low	Med	High
FPGA Interface Complexity	Low	Low	Med	High
Protocol Transparent	Yes	Yes	No	No
Protocols Supported	Aurora VITA 49 PCIe SRIO	Aurora VITA 49 PCIe SRIO	PCIe	SRIO

Figure 9

This table provides a side-by-side comparison of the four types of serial links we discussed in the previous pages and summarizes their main properties and supported protocols.

It can help the system designer narrow down the available links and protocols when evaluating the requirements of a proposed high-speed embedded system.

Switched Serial Fabrics

VXS: Switched Serial Fabric for VME

- VITA 41 Specification for 6U VMEbus
- Two Card Types Defined: Payload and Switch
- Payload Card
 - Processor, DSP, Memory, I/O, A/D, D/A, etc
 - Two 4x Serial Switched Fabric Ports on New P0 Connector
- Switch Card
 - Serial Fabric Crosspoint Switch
 - Joins Payload Cards via Backplane Wiring
- Base VITA 41.0 defines mechanical & electrical details
 - Completely independent of any serial protocol
- Protocol implementations are defined in sub-specifications

Figure 10

VXS is the popular name for a switched serial backplane fabric implementation for VMEbus.

Officially, it is being defined by the VITA standards organization as specification VITA 41. It defines two types of cards.

The VXS Payload Card is a processor, memory or I/O board, identical in concept to popular board functions already in use.

It has a new P0 connector that contains two 4X serial ports for data transfers across the backplane.

Each 4X serial port has four differential gigabit serial lines ganged together for input and another four serial lines for output, and they are commonly referred to as 4X serial ports.

Serial bit rates on each line are defined for frequencies up to 10 gigabits/second.

The VXS Switch Card is a new type of board with many serial ports and cross point switches to join the Payload cards.

The VXS specification is fabric-transparent, in that there are subspecifications, one for each of five fabrics.

VXS: Specification Status

- VITA 41.0
 - VXS Base Specification Approved
 - General info, mechanicals, connector, etc
- VXS Subspecifications

VITA 41.1	Infiniband Protocol Layer	Approved
VITA 41.2	Serial RapidIO Protocol Layer	Approved
VITA 41.3	Gigabit Ethernet	Draft
VITA 41.4	PCI Express	Draft
VITA 41.5	Aurora Protocol Layer	Draft
VITA 41.6	Gig-Ethernet Control Plane	Approved
VITA 41.7	VXS Processor Mesh	Draft
VITA 41.8	VXS 10 Gbit Enet Protocol	Draft
VITA 41.10	Live Insertion	Draft
VITA 41.11	Rear Transition Modules	Draft

Figure 11

As of this writing, the base specification that contains general information and the mechanical and connector specs has been approved.

Two protocols, the Infiniband and the Serial RapidIO have also been approved.

Two additional protocols, Gigabit Ethernet and PCI Express have been released in draft form. The Gig-Ethernet Control Plane spec was also approved, while the VXS Processor Mesh, VXS 10 Gbit Ethernet Protocol, Live Insertion, and Rear Transition Modules spec have all been released in draft form.



Switched Serial Fabrics

VXS Payload Card

- Typical functions: processor, CPU, memory, I/O
- Mechanically compatible with legacy VME boards
- Uses standard VME64x connector for P1 & P2
- Uses new MultiGig RT2 serial connector (between P1 & P2)
- Two Full-Duplex 4X Serial Ports: 1.25 GBytes/sec each

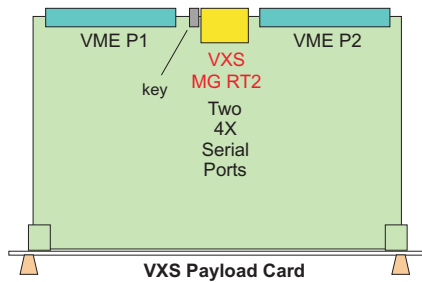


Figure 12

The VXS Payload card has a standard 6U VME outline with standard VME64x backplane connectors for P1 and P2.

You can see the new P0 backplane connector mounted between P1 and P2.

This is the new seven row Multi-Gig RT-2 connector for P0 and it handles two full duplex 4X serial ports.

VXS Switch Card

- Uses 6U VME board size
- No connection to VMEbus – instead five multiGig RT2
- Up to eighteen 4X serial ports to join VXS payload cards
- Up to four 4X serial ports to join other VXS switch cards
- Special backplane power connector and keying
- VXS backplane joins switch and payload boards

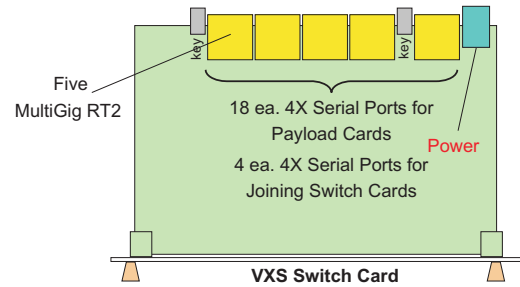


Figure 13

The VXS Switch card has a 6U VME board form factor but no P1 and P2 connectors.

Instead, it uses several Multi-Gig RT-2 connectors to handle up to eighteen 4X full-duplex switched serial ports.

This board joins the payload cards so they can talk to each other.

As you may already have guessed, we obviously need a new backplane.

Switched Serial Fabrics

Example: VXS Switch Card

- Connects to payload cards (18) and other switch cards (4)
 - Switch may be manual “fabric transparent” or automatic “protocol specific”
 - Optional links to copper or optical interfaces to networks or other chassis
- Switch cards may have any number of ports

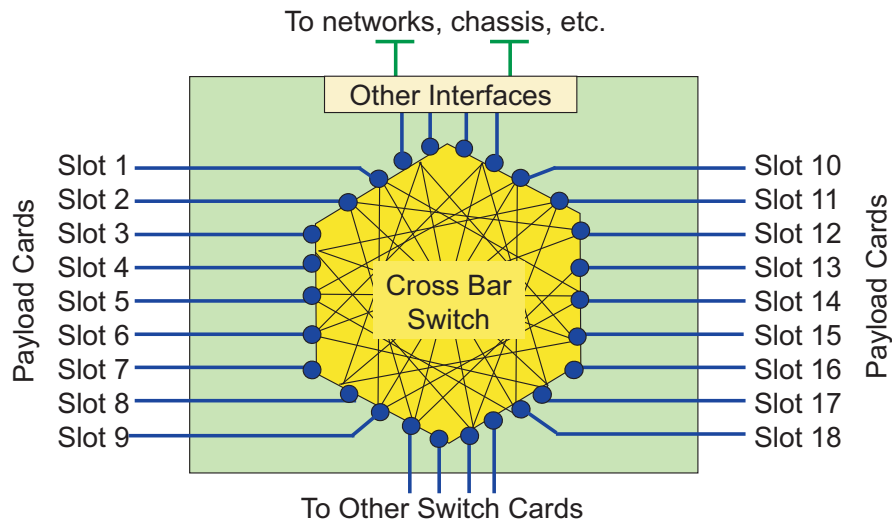


Figure 14

Looking inside just one example of a VXS switch card, we see a big cross point switch for handling traffic between payload boards.

We also see possible front panel connections to other interfaces like networks or storage devices.

With this architecture, any of the five fabrics can be used to deliver an incredibly well-connected solution for high-performance embedded systems.

Switched Serial Fabrics

Example: 20-slot VXS Dual Redundant Backplane

- MultiGig RT2 sockets are used for two 4X serial links
- One or two switch cards occupy special central slot(s)
- 4X links join every payload card to every other payload card via two paths

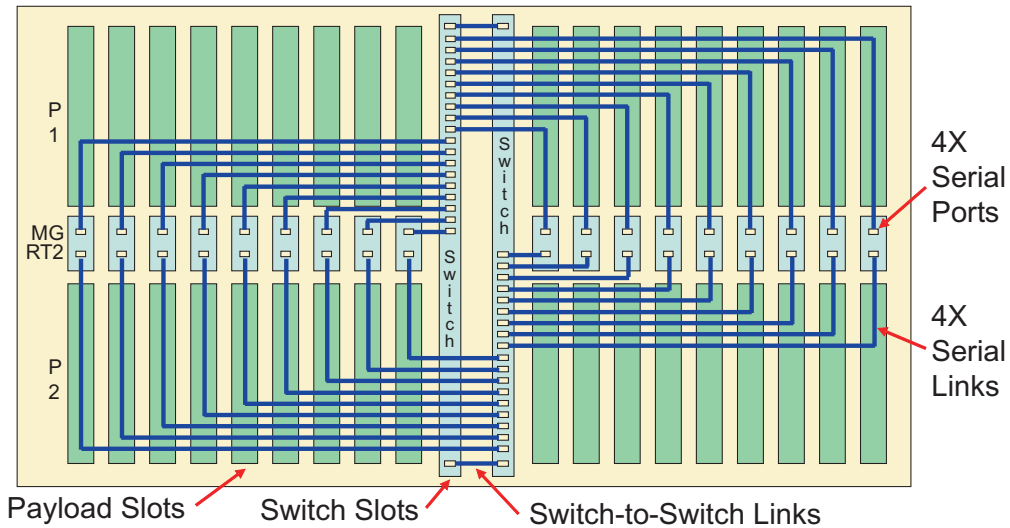


Figure 15

Here's a possible implementation of a 20-slot VXS backplane.

It has 18 payload slots, nine on the left and nine on the right. It also has two switch slots in the center.

The P0 connectors on the payload boards each have two 4X serial ports that are wired in copper through the backplane to the 4X serial ports on the switch boards.

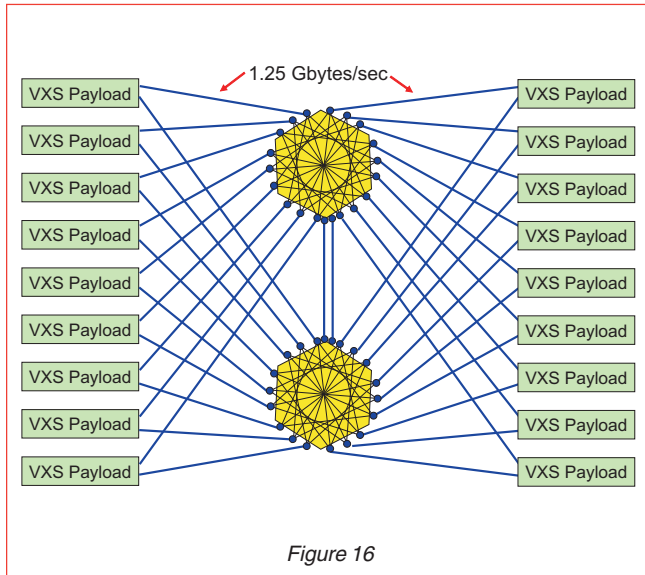
Notice there are two links between the switch boards so they can talk to each other as well.

This arrangement gives you two redundant serial links between every pair of boards in the cage.

And remember, unlike a bused backplane, all of these switched links can be operating at the same time.

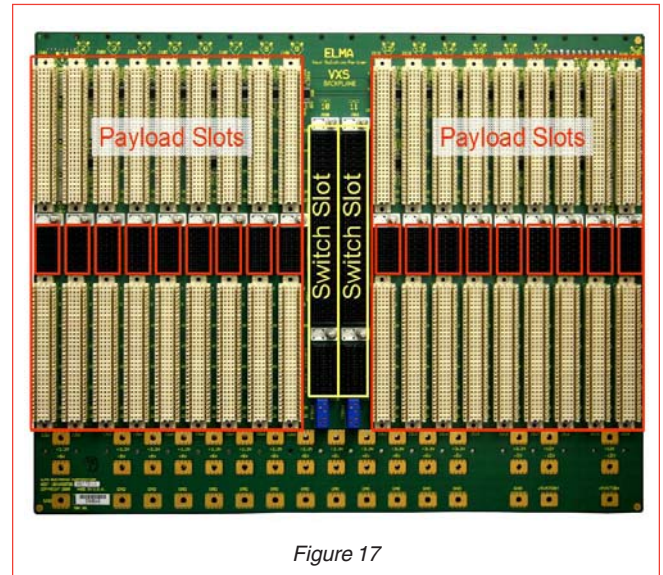
Switched Serial Fabrics

Example: 20-Slot VXS Dual Redundant Backplane



This diagram shows how the 18 payload cards connect to each switch card in the 20-slot backplane.

All 1.25 Gbytes/sec serial links are operating at the same time.



This is a photograph of the commercially available 20-slot VXS backplane with 18 payload cards and two switch cards.

Switched Serial Fabrics

XMC: Switched Serial Fabric for PMC

VITA Doc	Description	Status
42.0	Base Specification: connectors, mechanical, etc.	Approved
42.1	Parallel RapidIO	Approved
42.2	Serial RapidIO	Approved
42.3	PCI Express	Approved
42.4	HyperTransport	Draft
42.5	Aurora Pin Assignment	Tabled
42.6	XMC 10 Gbit Enet	Approved
42.10	General Purpose I/O	Draft

Figure 18

Defined under VITA 42, the XMC specification extends the PMC card by adding new connections to support gigabit serial interfaces plus a growing list of alternative I/O standards.

As shown in Figure 18, VITA 42.0 is the base specification that includes general information, reference and inheritance documentation, dimensional specifications, connectors, pin numbering and primary allocation of pairing and grouping of pin functions.

XMCs can be single- or double-width modules that use a pin-socket connector with 114 pins arranged in a 6 x 19 array. A single-width XMC can have one or two connectors with pin functions as shown in Figure 19. A double-width XMC can have up to four connectors.

To support gigabit serial interfaces, notice that both P15 and P16 connectors define 10 full-duplex differential pair lines. The VITA 42.0 base specification does not dictate signal types, data rates, protocols, voltage levels or grouping for these signals. Instead, it wisely leaves that up to the several subspecifications that follow, allowing XMCs to evolve as new standards emerge.

In fact, contrary to the fundamental mission of supporting serial interfaces, the first subspecification, VITA 42.1, defines these same pins for Parallel RapidIO. While VITA 42.1 is approved and fielded, few vendors

PMC/XMC Connector Definition

Each XMC Connector:
6 x 19 pin array
114 pins total

P16 Secondary XMC

P15 Primary XMC

(component side)

P15 Primary XMC Connector

- 10 differential pairs each direction
- JTAG
- System Management
- Auxiliary
- 3.3 V Power:
 - Main: 4 pins, 1 A/pin, 13.2 W
 - Auxiliary: 1 pin, for system management
- Variable Power
 - 8 pins, 1 A/pin
 - 5 V (40 W max) or 12 V (96 W max)
 - Modules must accept 5 V or 12 V
 - Carriers may provide 5 V or 12 V

P16: Secondary XMC Connector

- 10 more differential pairs each direction
- High-speed or single-ended user I/O
- Extensions of gigabit serial fabrics

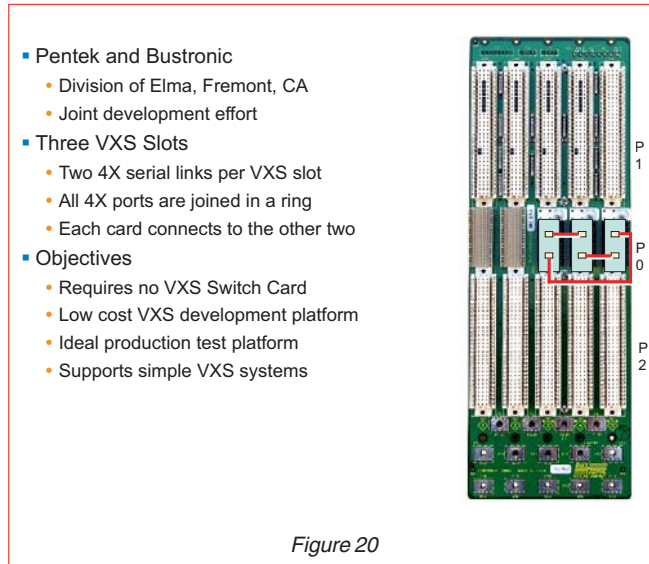
Figure 19

have embraced this standard and have instead opted for the more popular serial protocols.

As shown in Figure 19, most of the pins on P15 are reserved for serial links, power and other functions, but P16 has a wealth of user-defined pins now being addressed by the VITA 42.10 General Purpose I/O draft specification. It offers a standardized way of implementing interfaces for popular system I/O including Ethernet, USB ports, RS-232, RS-485, Serial ATA, Fibre Channel, and SAS (Serial Attached SCSI). The clear benefit here is that by following these definitions, XMC and carrier board designers can achieve a much wider range of interoperability, the essential goal of industry standards.

Switched Serial Fabrics

5-Slot Switchless VXS Backplane



Bustronic and Pentek jointly developed a simple, 5-slot VXS backplane that allows developers to get started with VXS technology without the need for a VXS switch card.

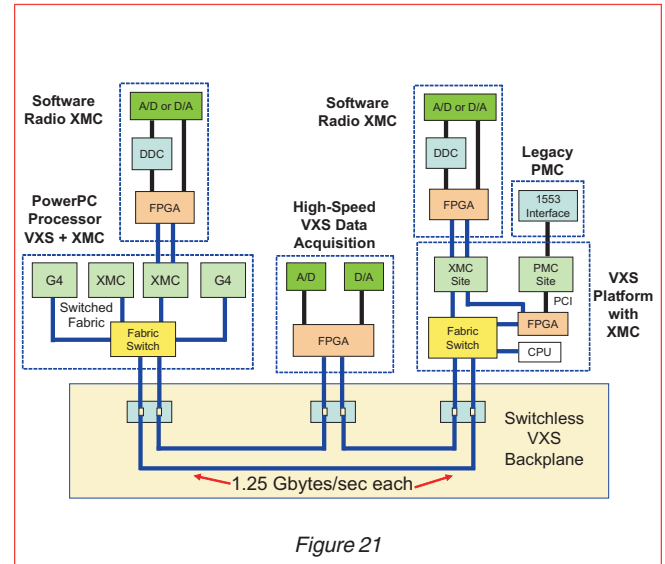
The backplane has three VXS payload slots and two legacy VME slots. All five slots share the common VMEbus.

Since there is no VXS switch card slot, the two 4X VXS links of each of the three VXS payload cards are joined together in a ring.

Each VXS card connects to the other two VXS cards through one dedicated 4X serial link capable of operating any protocol, including the Xilinx Aurora link layer protocol.

One benefit of this backplane is that it provides a low-cost development and product test platform for board vendors. It also provides system integrators with a low-cost platform for smaller systems with just a few cards that need extremely high-speed interconnects between the cards.

Switchless Backplane System



The system above, based on the switchless 5-slot VXS backplane, shows a PowerPC VXS board connected to a high-speed data acquisition VXS board and a VXS platform with both XMC and PMC module sites.

The PowerPC board has a software radio XMC module connected to its XMC site. The VXS platform has also an XMC software radio connected to its XMC module site and a legacy 1553 board connected to its PMC module site.

Each of the VXS link connections shown provides a full-duplex data path operating at speeds up to 1.25 GB/sec each.

We'll revisit this graphic at the end of the next section to discuss the role of the FPGAs in connection with switched serial fabrics.

Switched Serial Fabrics

VPX: VXS on Steroids

- Improves Number of Switched Fabric Ports over VXS
 - VXS uses only one MultiGig RT Connector – 2 gigabit serial 4x ports
 - VPX uses 3 to 7 MultiGig RT Connectors – 8 to 24 gigabit serial 4x ports
- Optional Switch Card
 - Most payload cards have switches on board
- 3U and 6U VME board form factors
 - IEEE 1101.1 and 1101.2
- Improves I/O Capacity
 - VME front panel I/O is restricted in military systems
 - Migrates to backplane connections for I/O
- Modernizes Power Distribution
 - Uses higher voltage on backplane with on-board power supplies
- Utilizes XMC Mezzanines
 - Maintains VITA 42 XMC Specification

Figure 22

By extending the use of gigabit serial links already proven under VXS, the embedded community created the VPX initiative, which was formally defined under VITA 46. As a migration from the earlier VME and VXS standards, VPX shares the same outline as 3U and 6U cards and supports XMC mezzanine modules defined under the VITA 42 standard.

While VXS allows only one MultiGig RTS connector on a 6U card, VPX extends that number to three for a 3U card and to seven for a 6U card. As a result, VPX payload cards support a much higher traffic bandwidth than VXS, with eight to 24 gigabit serial 4X ports compared to only two with VXS.

Like the VXS specification, the VITA 46.0 VPX base specification does not define backplane topologies or specific gigabit serial fabrics or protocols. As with VXS, implementations of each fabric protocol are defined as sub specifications, or “dot specs.”



VPX REDI

- REDI - Ruggedized Enhanced Design Implementation
- Defines Specific Mechanical Design Implementations for VPX
- Enhanced thermal management
 - Air, conduction, and liquid cooling
- Improved structural integrity
 - Cover plates to protect circuitry and ESD protection
- 2 Level Maintenance compatibility
 - Modules can be field swapped for field maintenance
- Dot Specifications Define Implementation Details
 - VITA 48.1 – REDI Air Cooling
 - VITA 48.2 – REDI Conduction Cooling
 - VITA 48.3 – REDI Liquid Cooling
 - VITA 48.5 – Air Flow Through Cooling

Figure 23

As industry started using VPX, a new extension emerged to deal with severe environmental requirements. The VITA 48 REDI (Ruggedized Enhanced Design Implementation) defines specific mechanical designs for enhanced thermal management using forced air, conduction cooling, and liquid cooling methods. It also defines protective metal covers for the cards to satisfy new requirements for simplified field servicing in deployed military applications.



Switched Serial Fabrics

3U VPX Board

- 3U board outline same as 3U VME
- P0 Utility Connector
 - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT-2 for P1 and P2 Signal Connectors
 - Definitions for differential or single-ended signals
 - Up to eight 4X gigabit serial ports
- One XMC mezzanine site

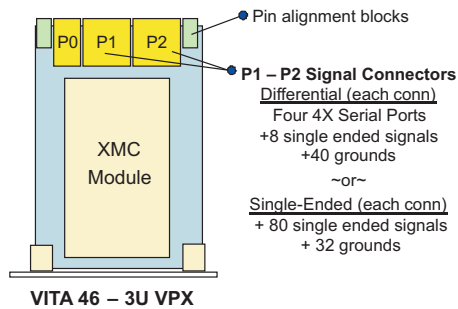


Figure 24

The 3U board outline is the same as the 3U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 3U board has two Multi-Gig RT2 Signal connectors, P1 and P2. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of eight 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 3U VPX board has one XMC mezzanine site that accepts one XMC module.

6U VPX Board

- 6U board outline same as 6U VME
- P0 Utility Connector
 - Power, system reset, reference clock, bus management, addressing, etc.
- MultiGig RT2 for P1 through P6 Signal Connectors
 - Definitions for differential or single-ended signals
 - Up to 24 4X gigabit serial ports
- One or two XMC mezzanine sites

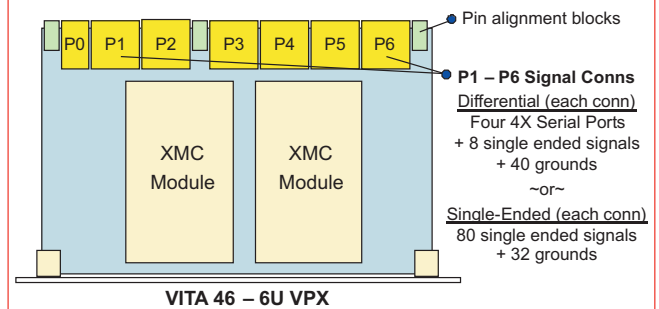


Figure 25

The 6U board outline is the same as the 6U VME board. The board has a P0 Utility connector which provides power, system reset, reference clock, addressing, bus management, and any other required utility functions.

The 6U board has six Multi-Gig RT2 Signal connectors P1 through P6. Each connector provides up to four 4X gigabit serial ports and this board offers a maximum of 24 4X ports. The VPX specification also defines how many signal and ground connections are available per signal connector.

The 6U VPX board has two XMC mezzanine site and accepts one or two XMC modules.

Switched Serial Fabrics

OpenVPX Initiative

- Rationale
 - To embrace VPX as a new system architecture, U.S. DOD mandated industry-wide definition and adoption of standards for VPX technology
 - Provide interoperability across vendors
 - Promote market priced components among competitors
 - Provide long-term availability for life-cycle support
- OpenVPX Industry Organization was formed in January 2009
 - 26 embedded system vendors, manufacturers and contractors
 - Goal: accelerate definition and turn over to VITA for standardization
- Transition to VITA Standard
 - Transferred to VSO (VITA Standards Organization) in October 2009
 - Designated as VITA 65
 - Ratified by VITA in February 2010
- ANSI Standardization
 - Received in June 2010

Figure 26

The OpenVPX organization was formed in January 2009 to promote industry-wide standards and long-term availability of VPX technology across the industry. The original VPX specification was being used, but because it permitted such a wide range of architectures, VPX systems tended to be unique, vendor-specific implementations.

The mission of OpenVPX was to enhance the original VPX standard by adding a set of well-defined system architectures, nomenclature and conventions to enable interoperability among vendors. Consisting of key vendors in the embedded-system community, all eager to convince government and military customers that VPX was suitable for current and future systems, the group made fast progress and turned over the completed specification to the VSO in October 2009 for standardization under VITA 65. In February 2010, the specification was ratified by VSO and ANSI approval was received in June 2010.



OpenVPX: VITA 65

- Defines sets of system implementations and system architectures
 - Promotes multi-vendor interoperability and life-cycle maintenance
 - Uses existing VITA 46 VPX Baseline and VITA 48 VPX REDI standards
- Defines various sizes of **pipes** used for serial communication
- Defines various **profiles** for structure and hierarchy:
 - slot profiles
 - backplane profiles
 - module profiles
 - development chassis profile
- Defines multiple **planes** for signal types within the specification:
 - Utility
 - Management
 - Control
 - Data
 - Expansion

Figure 27

OpenVPX defined new nomenclature for systems to describe the gigabit serial links in terms of the number of lanes and their function. The term “pipe” is used to define the number of bidirectional differential serial pairs that are grouped together to form a logical data channel.

OpenVPX also categorized the different kinds of traffic carried through the pipes as “planes”. The five planes defined are the utility, management, control, data and expansion planes.

In order to define architectural characteristics of systems, several “profiles” were defined. A slot profile specifies the pipes and planes found on the backplane connectors of each slot. The module profile specifies the pipes, planes, fabrics and protocols implemented on each card. The backplane profile defines how the slots are connected to each other by pipes. And finally, the development chassis profile includes the backplane profile and defines the dimensions, power supply, and cooling method.

Switched Serial Fabrics

OpenVPX Pipes

- Pipes
 - A grouping of differential pairs for an interconnect channel
 - Does not specify fabric protocols

Pipe Name	Abbreviation	# Diff Pairs	Also used
Ultra Thin Pipe	UTP	1	X1
Thin Pipe	TP	2	X2
Fat Pipe	FP	4	X4
Double Fat Pipe	DFP	8	X8
Quad Fat Pipe	QFP	16	X16
Octal Fat Pipe	OFP	32	X32



Figure 28

The OpenVPX Pipes are groups of differential pairs that are used to interconnect channels. As shown in the figure above, the defined OpenVPX pipe sizes range from one lane (1X) called an “ultra-thin pipe” or UTP, up to 32 lanes (32X) called an “octal fat pipe” or OFP.

The next size up from UTP is the “thin pipe” or TP which has two lanes or 2X. The popular 4X link is called a “fat pipe” or FP. The next size up from it is the “double fat pipe” or DFP with 8X links.

Next in size is the “quad fat pipe”, QFP or 16X and the fattest one is the “octal fat pipe”, OFP or 32X.

As used here and elsewhere in this handbook, the designation NX is the same as XN, or xN, where N is the number of lanes/pipes; The last designation, xN, is most commonly used with PCI Express.

OpenVPX Connector Layout

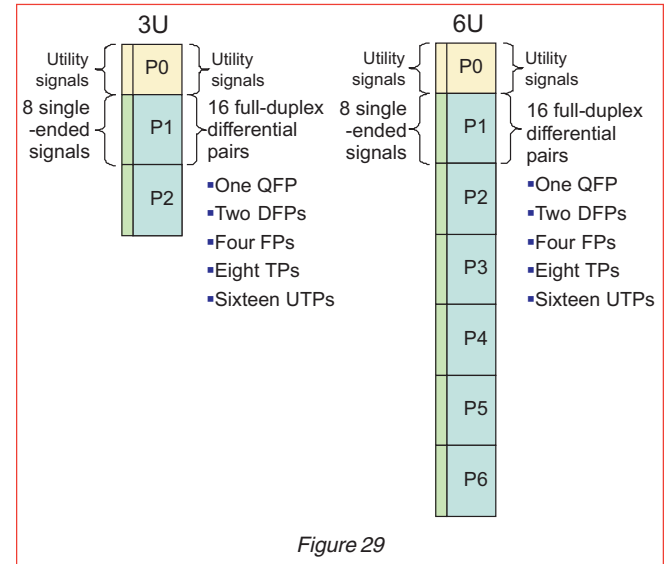


Figure 29

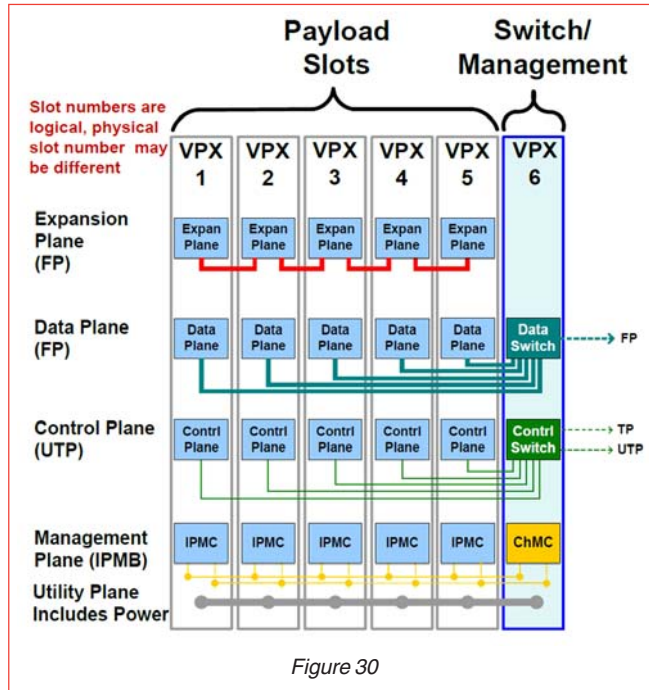
Shown here are the connector layouts for the 3U and 6U cards.

As shown previously, the 3U card has one utility connector for utilities such as power, clock, etc. It also has two signal connectors P1 and P2. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

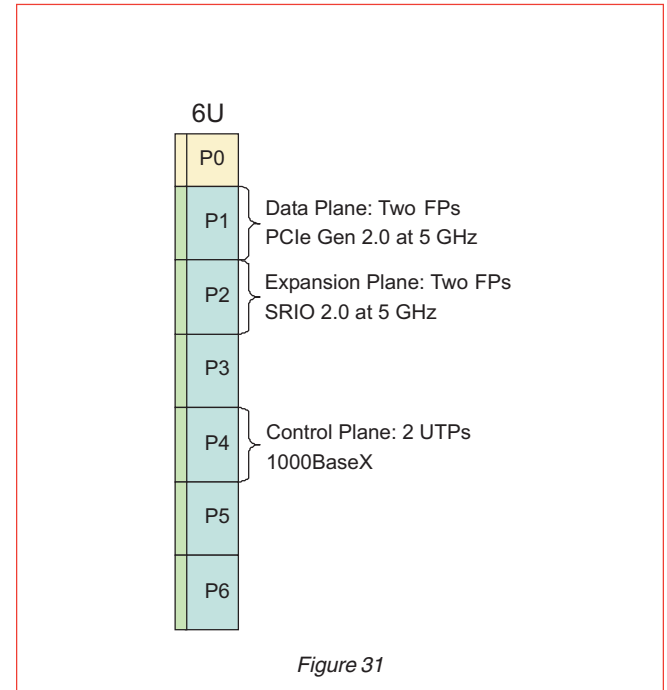
Likewise, the 6U board has the same utility connector and six signal connectors P1 through P6. Each of these provides connections for eight single-ended signals plus grounds. In addition, each one provides 16 full-duplex differential pairs with the following pipes: sixteen UTPs, eight TPs, four FPs, two DFPs and one QFP.

Switched Serial Fabrics

Typical OpenVPX Backplane Profile



Typical OpenVPX Module Profile



The OpenVPX specification established quite a large number of backplane profiles. The backplane profile is a physical definition of a backplane implementation. Included in this definition are:

- Slot sizes such as 3U or 6U
- Slot spacing such as 1.00, 0.85, or 0.80 inches
- Quantity of slots and type of slots
- Topologies used to interconnect the slots, such as:
 - ◆ Mesh
 - ◆ Central switch
 - ◆ Distributed
 - ◆ Root-leaf

Shown here is a typical 6-slot backplane with five payload cards and one switch/management card. Backplanes such as this one are primarily intended for development environments. However, some systems could be deployed in the field with these backplanes.

In addition to the backplane profiles, OpenVPX specifies module profiles. The module profile provides a physical mapping of ports into the module's backplane connectors. The module profile includes the assignment of specific protocols used for each port. It also provides first-order compatibility checks between modules and slots.

The typical module profile above shows the assignments for P1, P2, and P4. P0 is used for the utility functions. The assignments for the balance of connectors may be user-specified to suit the application.

Switched Serial Fabrics

VPX Specification Status

▪ VITA 46.0 – VPX Baseline Specification	Approved
• VITA 46.1 VMEbus Signal Mapping	Approved
• VITA 46.3 Serial RapidIO on VPX	Approved
• VITA 46.4 PCI Express on VPX	Approved
• VITA 46.6 Gbit Ethernet Control Plane on VPX	Draft
• VITA 46.7 Ethernet on VPX Fabric Connector	Approved
• VITA 46.8 Infiniband on the VPX Fabric Connector	Draft
• VITA 46.9 PMC/XMC Rear I/O to 3U/6U Pin Mapping	Approved
• VITA 46.10 Rear Transition Module for VPX	Approved
• VITA 46.11 System Management on VPX	Draft
• VITA 46.12 Fiber Optic Interconnect	Draft
• VITA 46.14 Analog R/F Interconnect	Draft
• VITA 46.20 VPX Switch Slot Definition	Draft
• VITA 46.21 Distributed Switching Topologies on VPX	Draft
▪ VITA 48.0 – REDI	Approved
• VITA 48.1 – REDI Air Cooling	Approved
• VITA 48.2 – REDI Conduction Cooling	Approved
• VITA 48.3 – REDI Liquid Cooling	Draft
• VITA 48.5 – Air Flow Through Cooling	Approved
▪ VITA 65 – OpenVPX	Approved
• VITA 65.0 Base Specification	Approved
▪ VITA 66 – Optical Interconnect on VPX	Approved
• VITA 66.0 Optical Interconnect on VPX, Base Spec	Approved
• VITA 66.1 Optical Interconnect on VPX, MT Variant	Approved
• VITA 66.2 Optical Interconnect on VPX, Airinc Variant	Approved
• VITA 66.3 Optical Interconnect on VPX, Beam Variant	Approved
▪ VITA 67 – Coaxial Interconnect on VPX	Approved
• VITA 67.0 Coaxial Interconnect on VPX, Base Spec	Approved
• VITA 67.1 Coaxial Interconnect on VPX, 3U	Approved
• VITA 67.2 Coaxial Interconnect on VPX, 6U	Approved
• VITA 67.3 Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	Draft

Figure 32

As of this writing, the VPX Baseline Specification has been approved by both VITA and ANSI and has been released as VITA 46.0

Also approved by VITA and ANSI and released is VITA 46.1 the VMEbus Signal Mapping, Vita 46.3 the Serial RapidIO on VXS, Vita 46.4 PCI Express on VPX, VITA 46.7 Ethernet on VPX Fabric Connector, VITA 46.9 the PMC/XMC Rear I/O Pin Mapping and 46.10 the Rear Transition Module for VPX. The balance of the VITA 46 subspecifications are in draft form.

Likewise, the VITA 48.0 REDI is approved. Also approved are all of its subspecifications except for Liquid Cooling which is in draft form.

Also, the OpenVPX VITA 65.0 Base Specification has been approved by VITA and ANSI.

Two more VITA standards have been approved: VITA 66.0 Optical Interconnect on VPX and VITA 67.0 Coaxial Interconnect on VPX. The latter was initiated by DRS. Pentek has been actively involved in the development of this specification.

VITA 67.3 Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane has been released in draft form.

For more information regarding VITA/ANSI standards, contact:

VMEbus International Trade Association

<http://www.vita.com>



FPGA Resources

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
 - Control logic
 - Glue logic
 - Registers and gates
 - State machines
 - Counters and dividers
- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

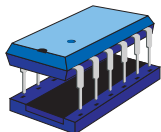


Figure 33

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
 - Schematic processors
 - Boolean processors
 - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
 - Critical paths and propagation delays
 - Pin assignment and pin locking
 - Signal loading and drive capabilities
 - Clock distribution
 - Input signal synchronization and skew analysis



Figure 34

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

FPGA Resources

FPGAs: New Device Technology

- ◆ 500+ MHz DSP slices and memory structures
- ◆ Over 3500 dedicated on-chip hardware multipliers
- ◆ On-board GHz serial transceivers
- ◆ Partial reconfigurability maintains operation during changes
- ◆ Switched fabric interface engines
- ◆ Over 690,000 logic cells
- ◆ Gigabit Ethernet media access controllers
- ◆ On-chip 405 PowerPC RISC microcontroller cores
- ◆ Memory densities approaching 85 million bits
- ◆ Reduced power with core voltages at 1 volt
- ◆ Silicon geometries to 28 nanometers
- ◆ High-density BGA and flip-chip packaging
- ◆ Over 1200 user I/O pins
- ◆ Configurable logic and I/O interface standards



Figure 35

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you'll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking below 0.1 micron.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

FPGAs: New Development Tools

- High Level Design Tools
 - Block Diagram System Generators
 - Schematic Processors
 - High-level language compilers for VHDL & Verilog
 - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
 - Faster compilers and simulators save time
 - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
 - FPGA vendors offer both free and licensed cores
 - FPGA vendors promote third party core vendors
 - Wide range of IP cores available



Figure 36

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

FPGA Resources

FPGA Resource Comparison

	Virtex-II Pro VP	Virtex-4 FX, LX, SX	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX
Logic Cells	53K–74K	55K–110K	52K–155K	128K–314K	326K–693K
Slices*	23K–33K	24K–49K	8K–24K	20K–49K	51K–108K
CLB Flip-Flops	46K–66K	48K–98K	32K–96K	160K–392K	408K–864K
Block RAM (kb)	4,176–5,904	4,176–6,768	4,752–8,784	9,504–25,344	27,000–52,920
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E	DSP48E
DSP Slices	232–328	96–512	128–640	480–1,344	1,120–3,600
Serial Gbit Transceivers	N/A	0–20	12–16	20–24	28–80
PCI Express Support	N/A	N/A	N/A	Gen 2 x8	Gen 2 x8, Gen 3 x8
User I/O	852–996	576–960	480–680	600–720	700–1,000

*Virtex-II Pro and Virtex-4 Slices actually represent 2.25 Logic Cells;
 *Virtex-5, Virtex-6 and Virtex-7 Slices actually represent 6.4 Logic Cells

Figure 37

The above chart compares the available resources in the five Xilinx FPGA families that are used in most of the Pentek products.

- Virtex-II Pro: VP
- Virtex-4: FX, LX and SX
- Virtex-5: LX and SX
- Virtex-6: LX and SX
- Virtex-7: VX

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

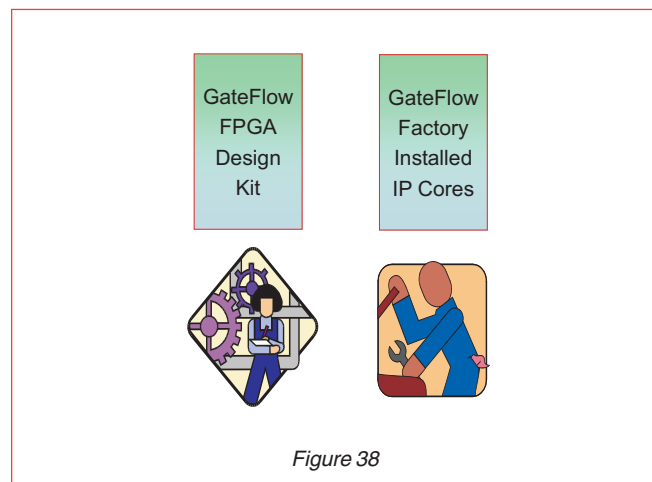
The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 500 MHz in V-4, to 550 MHz in V-5, to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.

FPGA Resources

GateFlow FPGA Design Resources



GateFlow® is Pentek's flagship collection of FPGA Design Resources. The GateFlow line is compatible with the Xilinx Virtex products and is available as two separate offerings:

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

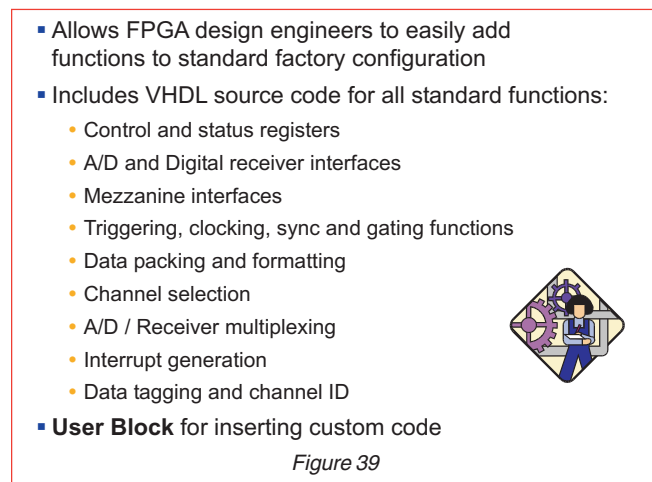
We also offer popular high-performance signal-processing algorithms with the GateFlow factory-installed IP Cores. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products

Installed Cores are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully supported with Pentek ReadyFlow® Board Support Packages.

Let's start with the GateFlow FPGA Design Kit.



GateFlow FPGA Design Kit



If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

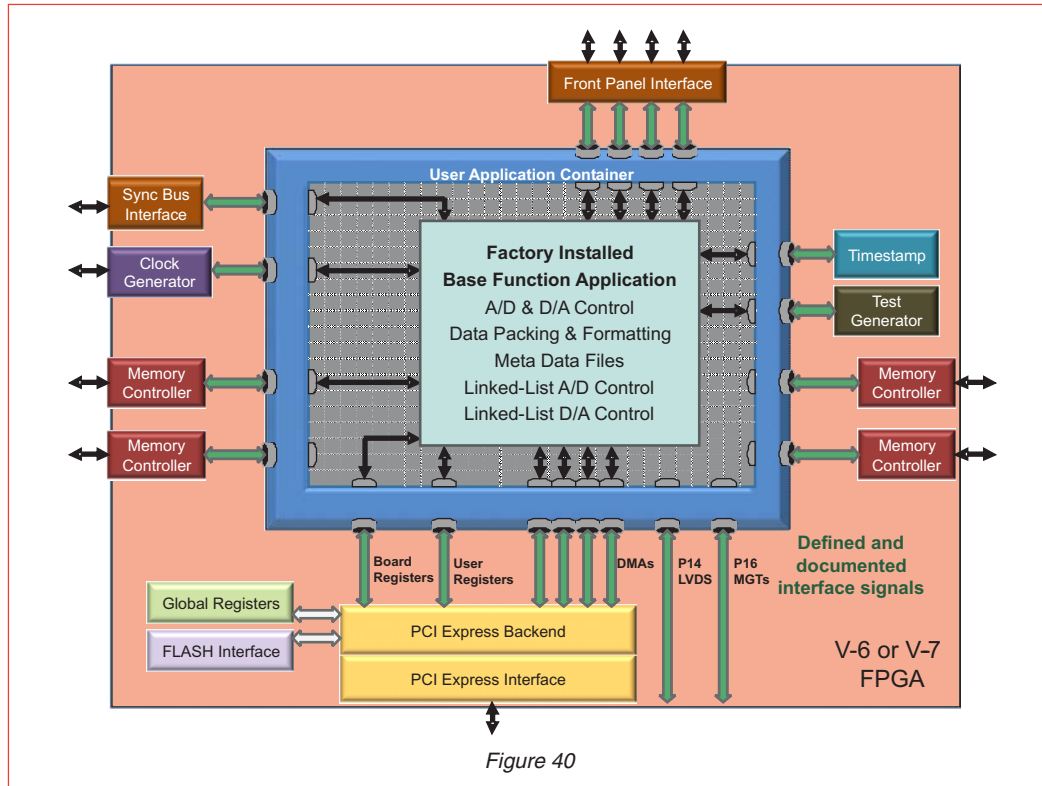
This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, and data tagging.

These are also fully supported with our ReadyFlow Board Support Package.

We also include a special User Block, positioned right in the data stream, so you can easily drop in your own custom signal processing algorithms.

FPGA Resources

GateFlow FPGA Design Kit for Cobalt or Onyx Products



The GateFlow FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt and Onyx architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

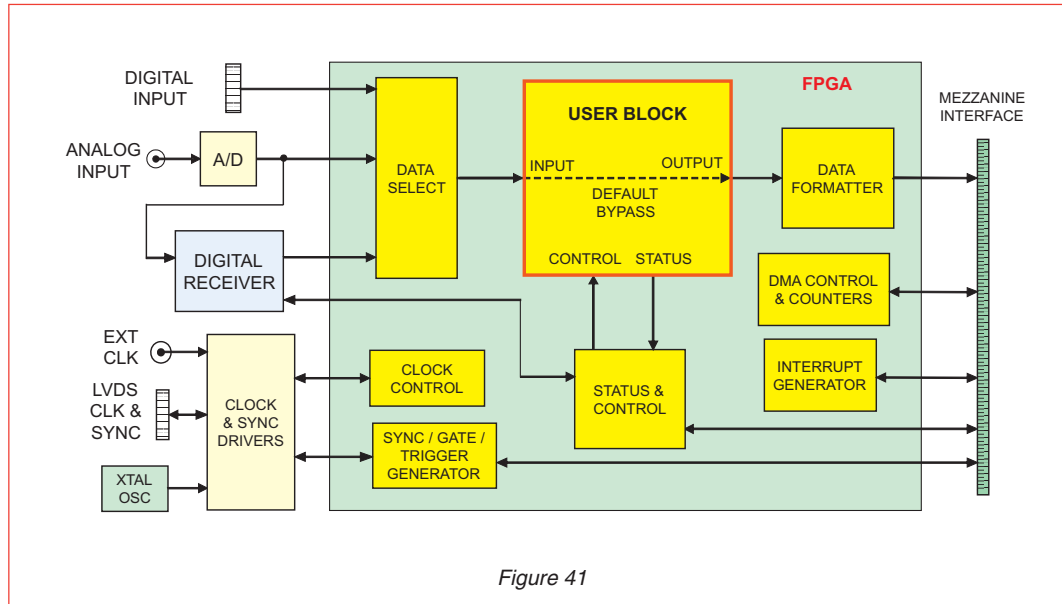
Shown here is the FPGA block diagram of a typical Cobalt or Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



FPGA Resources

GateFlow FPGA Design Kit for Other Pentek Products



The GateFlow FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

Shown above is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it.


The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.




FPGA Resources

GateFlow Installed IP Cores



- Pentek Installs IP Cores in Pentek Products
- Cores are tailored and optimized for:
 - Specific devices and I/O found on Pentek products
 - Efficient FPGA resource utilization
 - Execution and throughput speed
- Eliminates need for customer FPGA development
- Fully supported with ReadyFlow Board Support Libraries



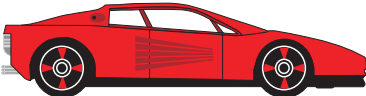


Figure 42

Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

Pentek offers popular high-performance signal processing algorithms installed in Pentek products. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products. The cores take full advantage of the numerous hardware multipliers to achieve highly-parallel processing structures that can dramatically outperform programmable RISC and DSP processors.

Installed Cores are optimized for efficient FPGA resource utilization, execution and throughput speed. They are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully tested and supported with the Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.



FPGA Resources

VXS and XMC: Extreme Connectivity through FPGA-based Interfaces

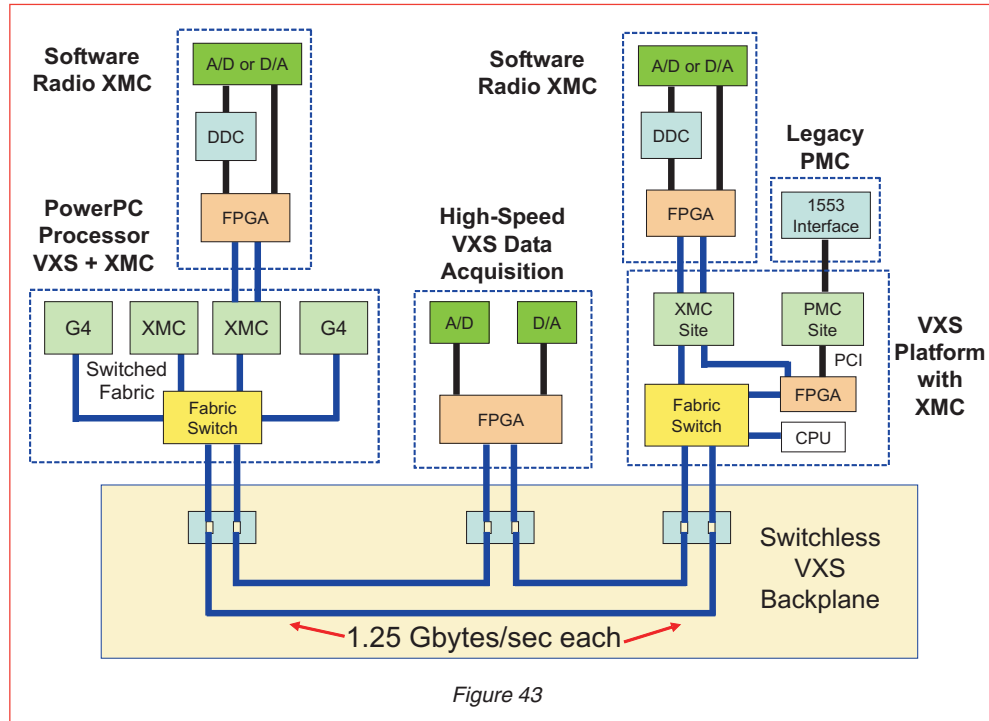


Figure 43

Figure 43 depicts a high-speed data acquisition and analysis system that utilizes products with VXS and XMC, the switched serial fabrics we presented in the opening section of this handbook. These interfaces are implemented within the FPGAs of the products in this system which utilizes the switchless VXS backplane.

Starting at the top left, we have a software radio XMC mezzanine that connects to a G4 PowerPC processor board via an XMC interface implemented in its on-board FPGA. The processor board itself is equipped with an XMC site and connects to the switchless backplane via the VXS interface of the on-board fabric switch.

Next, we have a high-speed A/D and D/A converter board that connects to the backplane via VXS which is implemented in its on-board FPGA.

We also have a second software radio XMC mezzanine that connects to a VXS platform equipped with XMC and PMC sites; the XMC interface is implemented in its on-board FPGA.

A legacy PMC 1553 mezzanine is also connected to the VXS platform via its PMC site and transfers data to the fabric switch through the connection implemented in the FPGA of the VXS platform.

In the next section, we will introduce you to Pentek products with extreme connectivity: products that can be used to create systems such as this.

Products

PMC, XMC, CompactPCI, PCI, PCI Express, OpenVPX, AMC, and VME/VXS Analog I/O Products

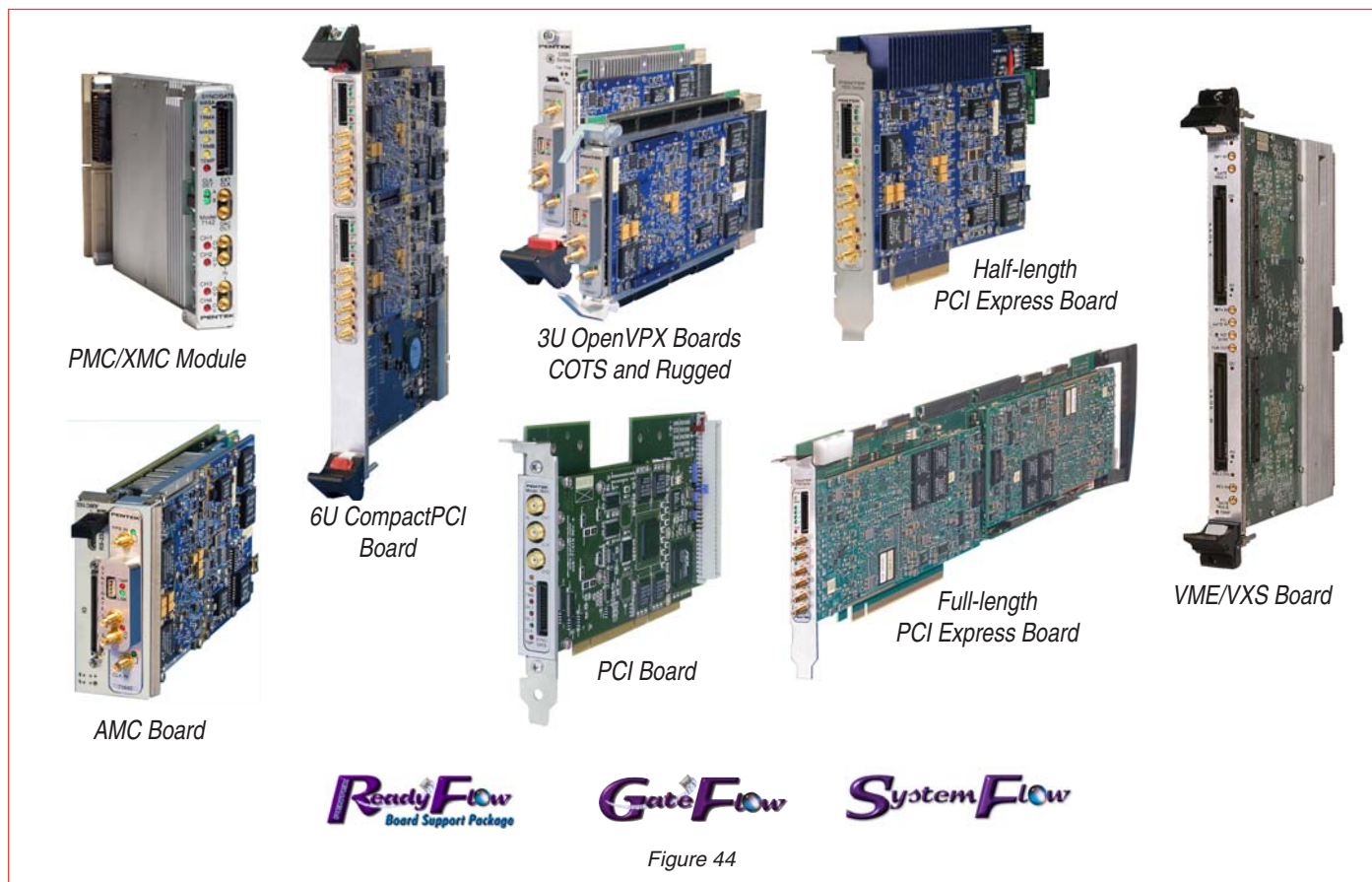


Figure 44

The Pentek family of board-level analog I/O products is the most comprehensive in the industry. Most of these products are available in several formats to satisfy a wide range of requirements.

In addition to their commercial versions, many of these products are available in ruggedized and conduction-cooled versions.

All of the analog I/O products include input A/D converters. Some of these products are also software radio receivers in that they include DDCs. Others are software radio transceivers because they include DDCs as well as DUCs with output D/A converters. These come with independent input and output clocks.

All Pentek analog I/O products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow[®] Board Support Package, the GateFlow[®] FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek board-level products. In addition, Pentek recording systems are supported with SystemFlow[®] recording software that features a Windows[®] graphical user interface.

In addition to product overviews presented in the pages that follow, a complete listing of these products with active links to their datasheets on Pentek's website is included at the end of this handbook.

Products

MPC8641D PowerPC Processor with Virtex-4 FPGA - VME/VXS

Model 4207

- MPC8641 single or dual core PowerPC processor to 1.5 GHz
- Xilinx Virtex-4 FX Series FPGA
- Hosts two PMC or XMC modules
- On-board dual gigabit Ethernet interfaces
- Optional on-board 4-Gbit dual optical Fibre Channel controller
- Optional dual optical gigabit serial Fibre Channel interface
- Up to 2 GB DDR2 SDRAM
- Two 64-bit PCI-X buses
- VME64x master/slave interface
- Optional VXS interface
- **Ruggedized and conduction-cooled versions**

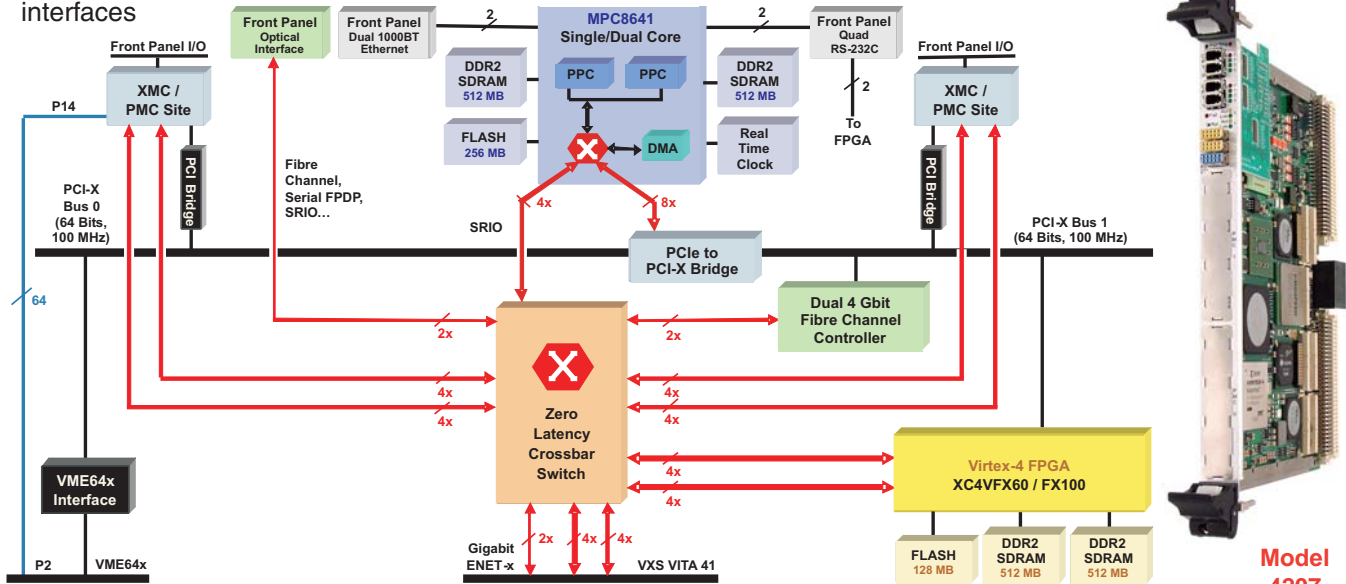


Figure 45

The Pentek Model 4207 PowerPC® VME/VXS I/O processor board targets embedded applications that require high-performance I/O and processing. With two PMC/XMC module sites, the 4207 offers powerful one-slot solutions with nearly unlimited high-speed connectivity.

Utilizing a unique crossbar switch architecture, the 4207 allows you to make the connections you want between board resources and high-speed interfaces. You don't need hardwiring, or FPGA space to define your I/O data flow and resource assignment.

The Freescale® MPC8641 utilizes the AltiVec® engine to perform parallel processing of multiple data elements (SIMD) with 128-bit operations. The AltiVec processor executes both fixed- and floating-point instructions. It is available with either single or dual e600 PowerPC core with maximum clock frequency of 1.5 GHz.

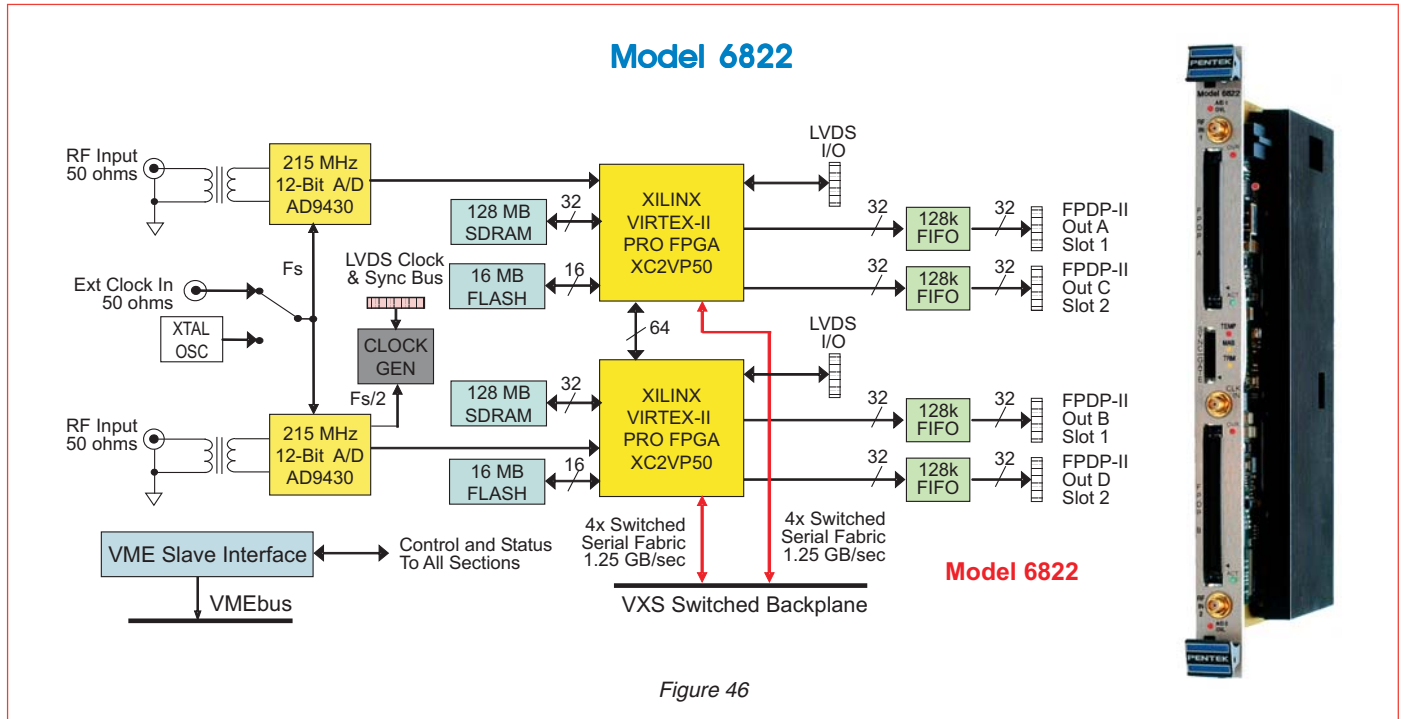
The 4207 may be optionally equipped with a Xilinx Virtex-4 FX FPGA, either the XC4VFX60 or the XC4VFX100. Two 4X RocketIO ports provide high-speed serial data paths to and from the FPGA.

Unused FPGA resources are available for the user to implement custom signal-processing configurations and algorithms using Pentek's GateFlow FPGA Design Kit and the high-performance IP Core Library.

The Model 4207 is supported with world-class software for initialization, control and optimization. In addition to GateFlow, this includes real-time OS support for VxWorks and Linux, ReadyFlow board support package and VSIPL scientific and engineering functions.

Products

Dual 215 MHz, 12-bit A/D with Virtex-II FPGAs - VME/VXS



The Model 6822 is a 6U single slot board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

Optional 4X switched serial fabric ports, compliant with the VITA 41 VXS backplane fabric standard, deliver data to VXS devices using two full-duplex 1.25 GB/sec data ports.

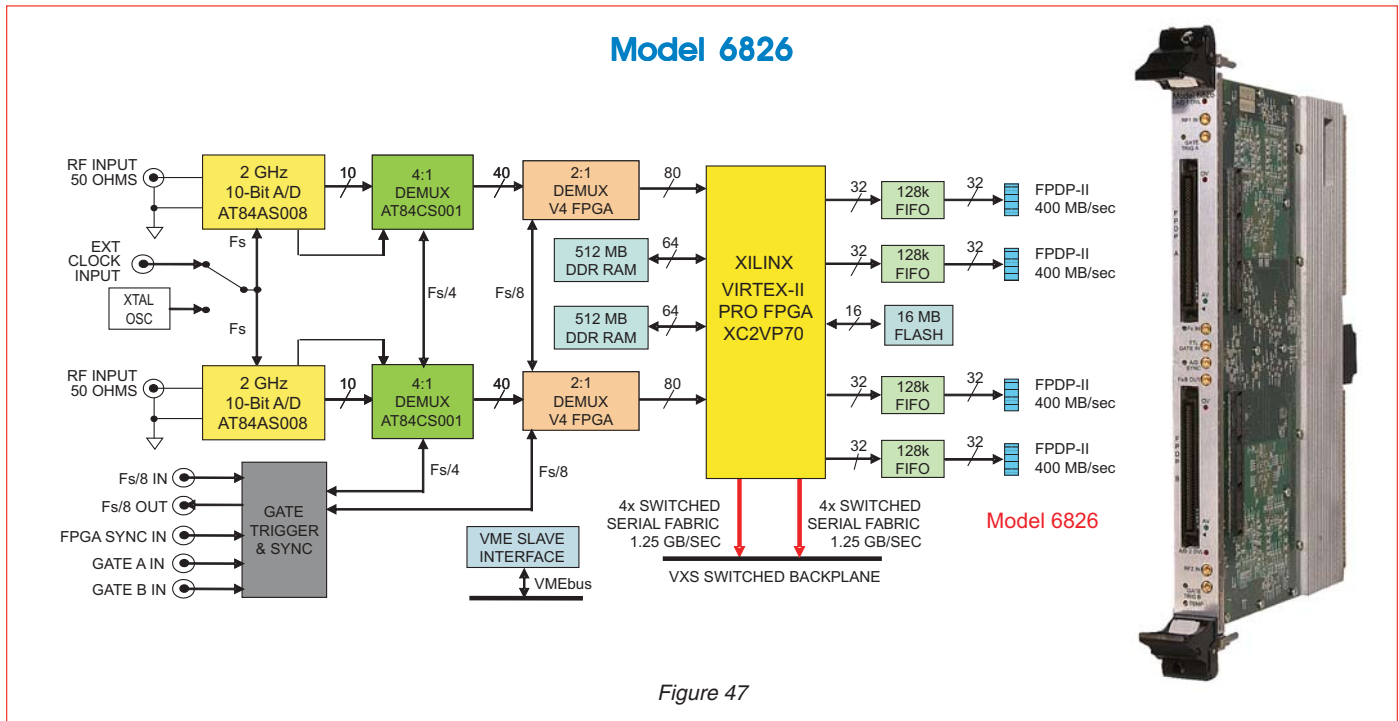
Since the switched fabric interface is implemented using the Rocket I/O gigabit serial transceivers in the FPGAs, the Model 6822 can support any of the switched fabric protocols including Serial RapidIO, PCI Express, or the lightweight point-to-point link layer protocol Aurora.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.

Products

Dual 2 GHz A/D with Xilinx Virtex-II Pro FPGA - VME/VXS



The Model 6826 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital

filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGA to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGA over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

The 400 MB/sec FPDP ports run out of speed at an A/D sample rate of 1.6 GHz for one channel.

With VXS, however, the two 1.25 GB/sec ports can maintain continuous streaming data at up to 2.5 GB/sec, nicely handling the full 2 GHz A/D speed for one channel.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.

Products

Multichannel Transceivers with Virtex-4 FPGAs

**Model 7142 PMC/XMC • Model 7242 6U cPCI • Model 7342 3U cPCI • Model 7642 PCI
Model 7742 Full-length PCIe • Model 7842 Half-length PCIe • Model 5342 3U VPX**

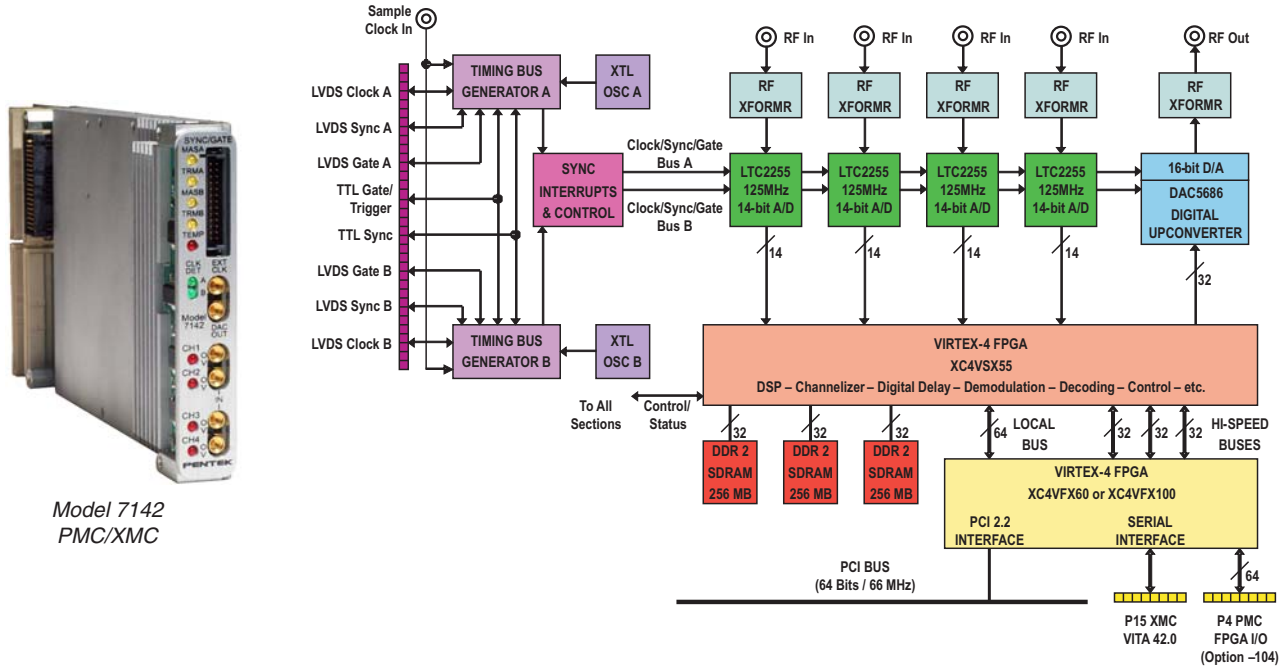


Figure 48

The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

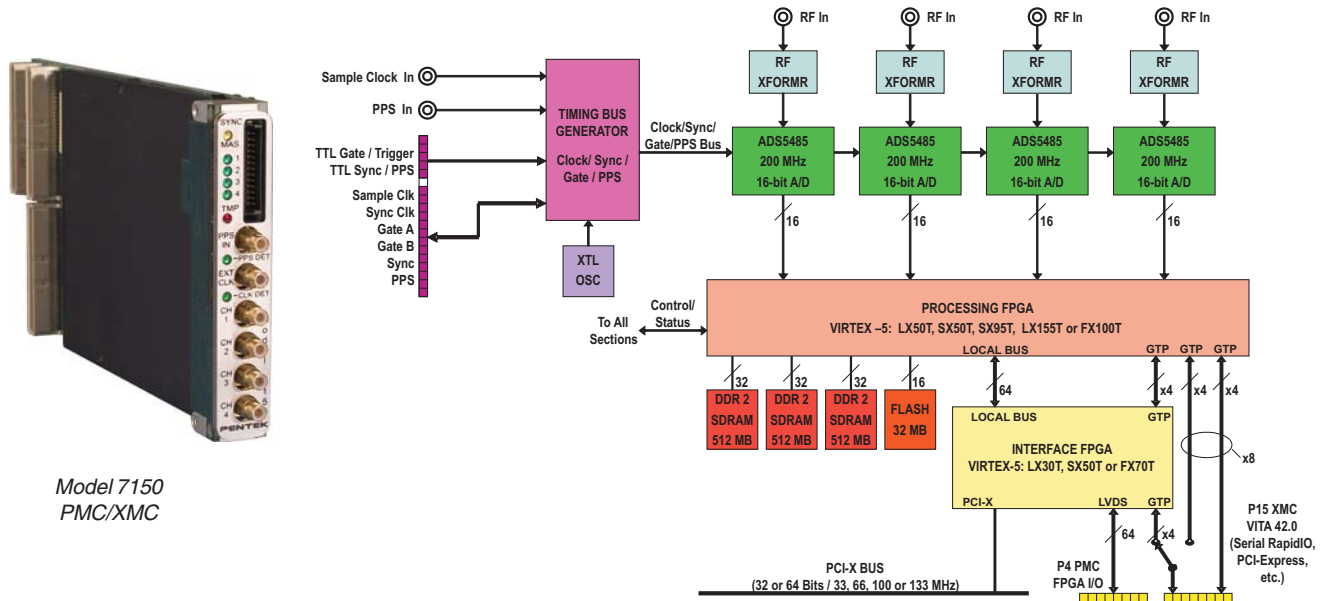
A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe full-length board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), 3U VPX (Model 5342), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).

Products

Quad 200 MHz 16-bit A/D with Virtex-5 FPGAs

**Model 7150 PMC/XMC • Model 7250 6U cPCI • Model 7350 3U cPCI • Model 7650 PCI
Model 7750 Full-length PCIe • Model 7850 Half-length PCIe • Model 5350 3U VPX**



Model 7150
PMC/XMC

Figure 49

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems. Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched fabric interfaces.

The Model 7150 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Three independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient

capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 9-channel DMA controller and 64 bit / 133 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7150 are also available as a PCIe full-length board (Models 7750 and 7750D dual density), PCIe half-length board (Model 7850), PCI board (Model 7650), 6U cPCI (Models 7250 and 7250D dual density), 3U cPCI (Model 7350), and 3U VPX (Model 5350).

Products

Dual 400 MHz 14-bit A/D and 800 MHz D/A with Virtex-5 FPGAs

**Model 7156 PMC/XMC • Model 7256 6U cPCI • Model 7356 3U cPCI • Model 7656 PCI
Model 7756 Full-length PCIe • Model 7856 Half-length PCIe • Model 5356 3U VPX**

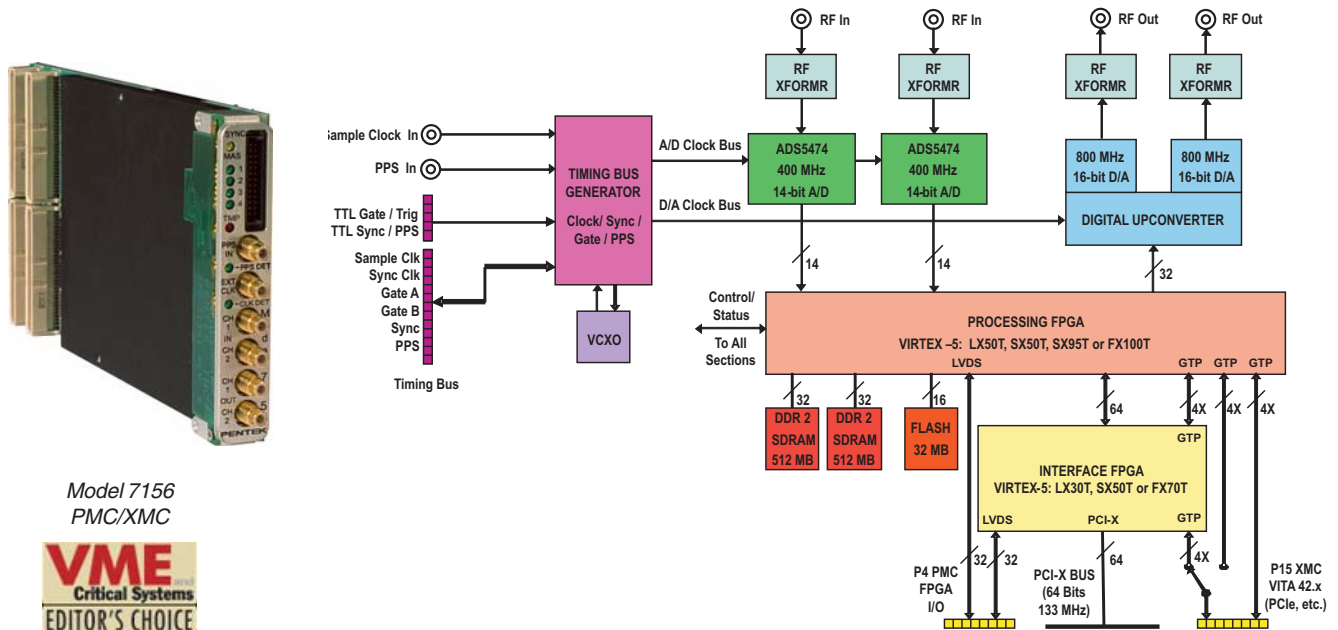


Figure 50

Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 133 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe full-length board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), 3U cPCI (Model 7356), and 3U VPX (Model 5356). All these products have similar features.

Products

Dual 500 MHz 12-bit A/D and 800 MHz D/A with Virtex-5 FPGAs

**Model 7158 PMC/XMC • Model 7258 6U cPCI • Model 7358 3U cPCI • Model 7658 PCI
Model 7758 Full-length PCIe • Model 7858 Half-length PCIe • Model 5358 3U VPX**

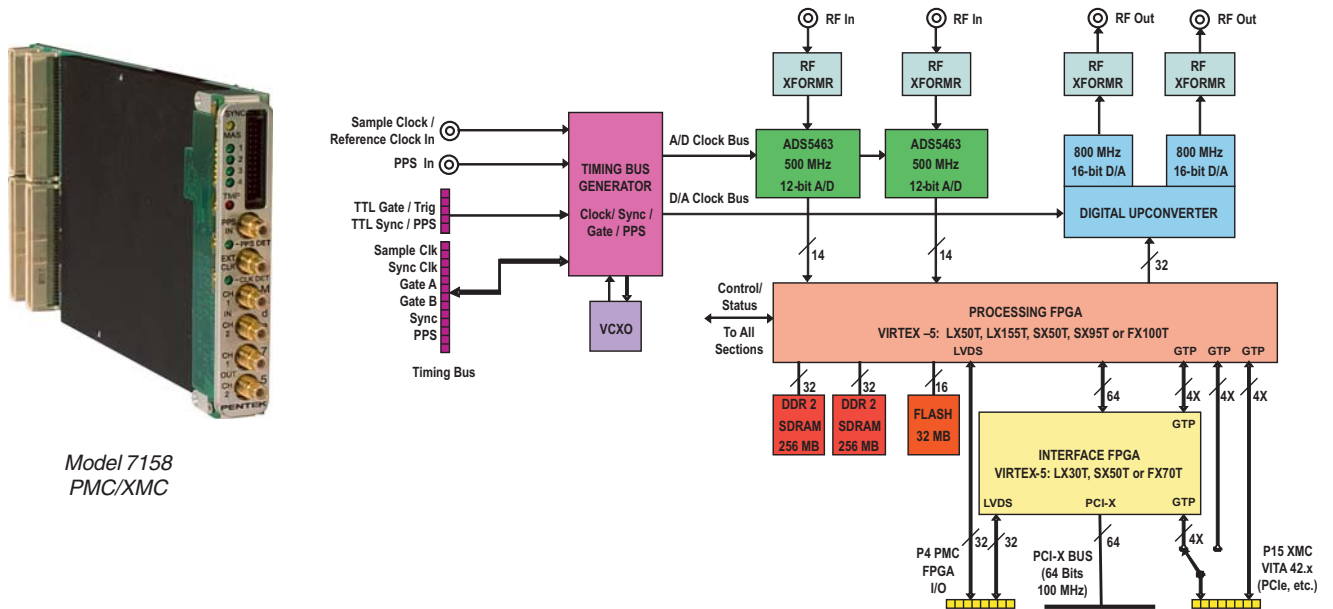


Figure 51

Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe full-length board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), 3U cPCI (Model 7358), and 3U VPX (Model 5358). All these products have similar features.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

**Model 71620 XMC • Model 78620 PCIe • Model 52620 3U VPX • Model 53620 3U VPX
Model 56620 AMC • Model 72620 6U cPCI • Model 73620 3U cPCI • Model 74620 6U cPCI**

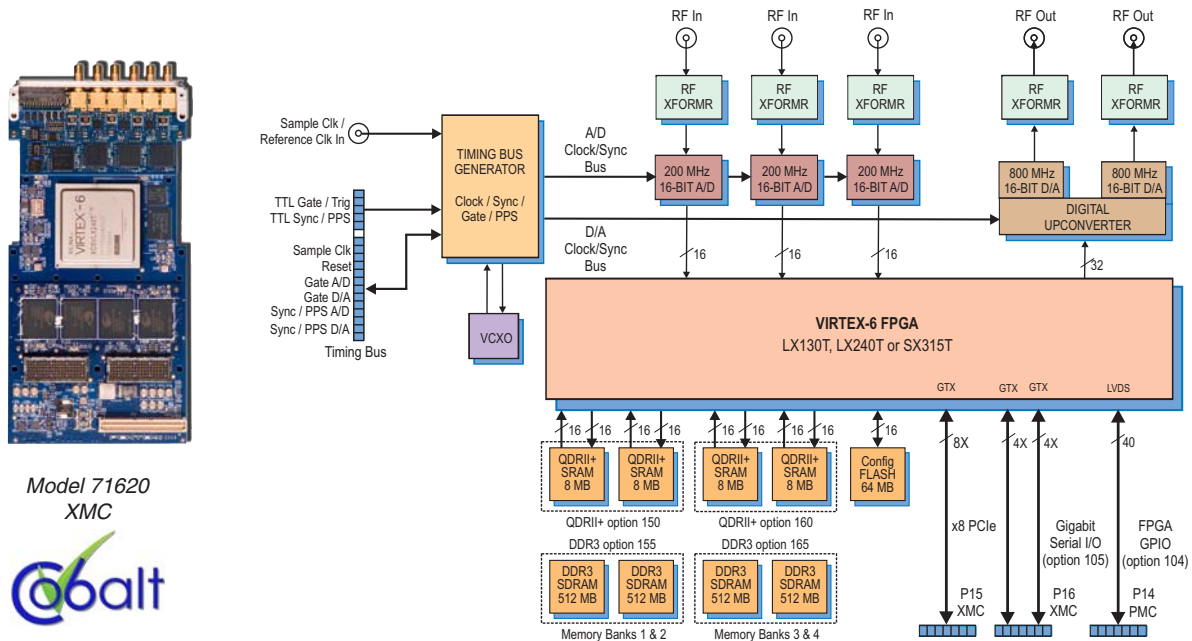


Figure 52

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71620 are also available as a PCIe half-length board (Model 78620), 3U VPX (Models 52620 and 53620), AMC (Model 56620), 6U cPCI (Models 72620 and 74620 with dual density), and 3U cPCI (Model 73620).

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

**Model 71720 XMC • Model 78720 PCIe • Model 52720 3U VPX • Model 53720 3U VPX
Model 56720 AMC • Model 72720 6U cPCI • Model 73720 3U cPCI • Model 74720 6U cPCI**

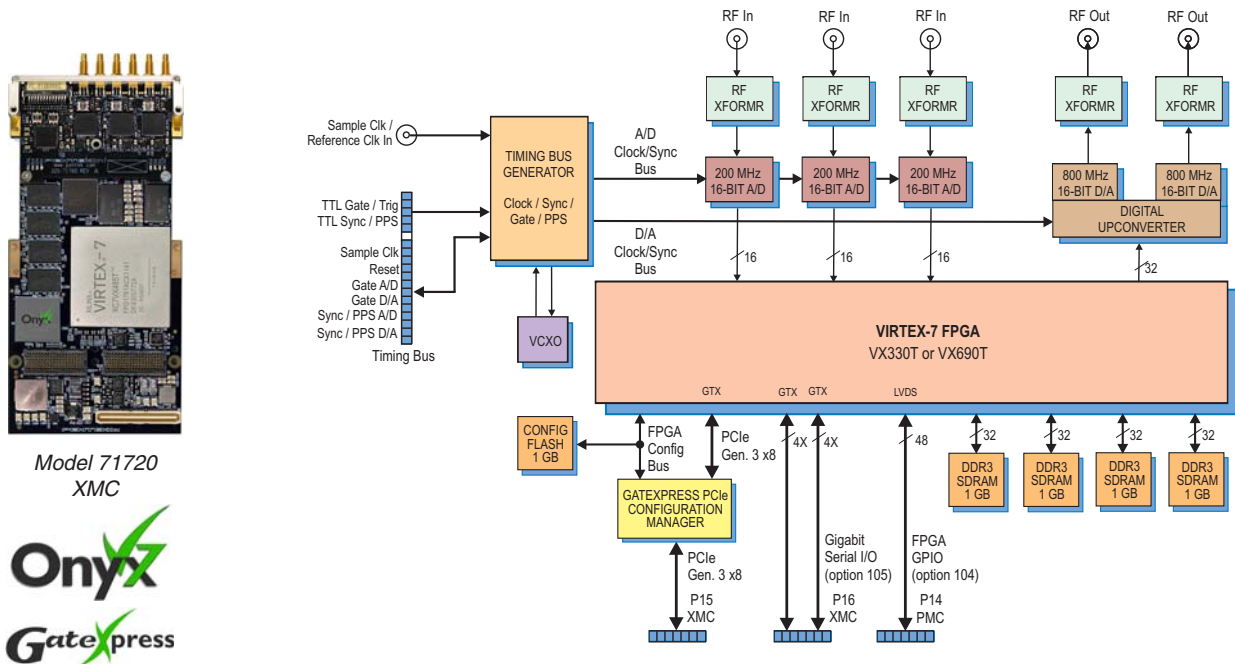


Figure 53

Model 71720 is a member of the Onyx[®] family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

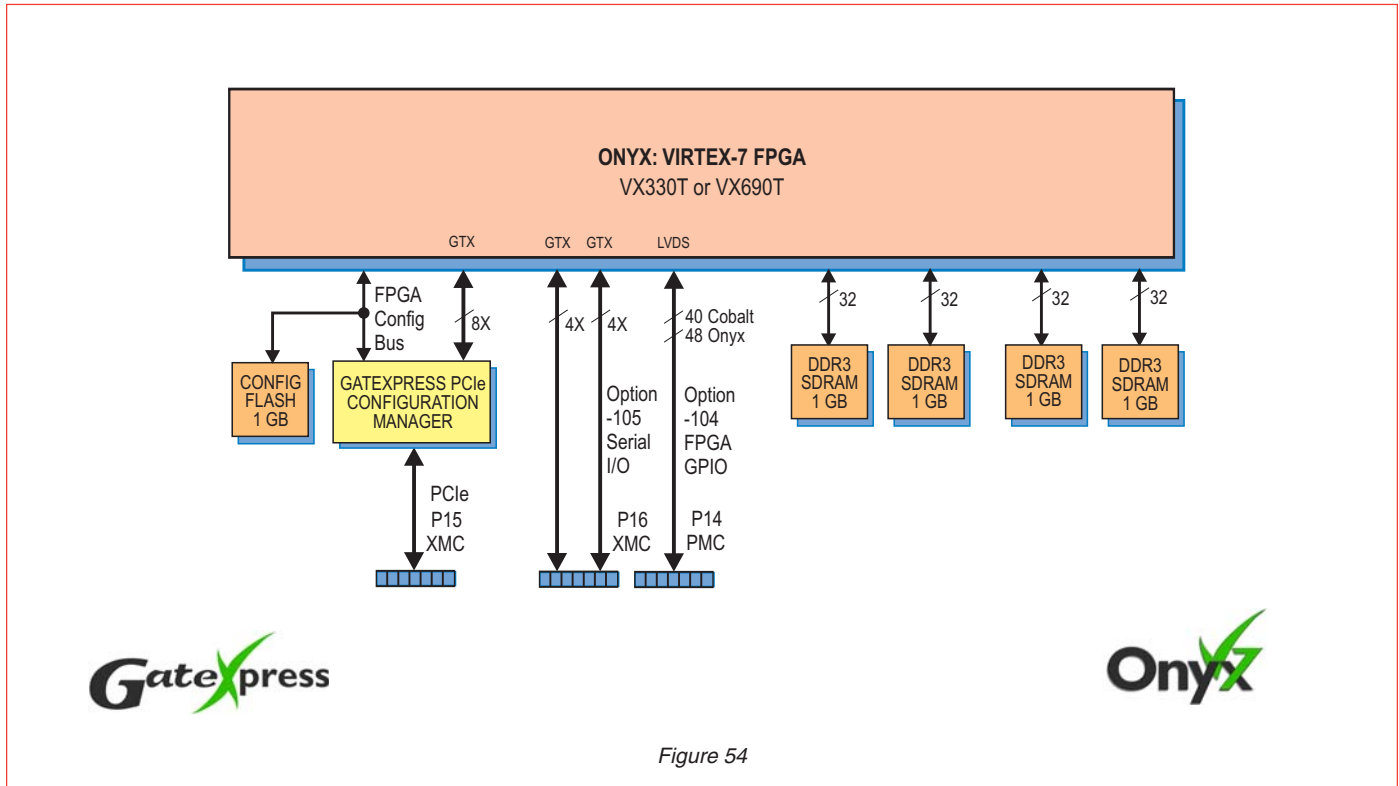
Multiple 71720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Versions of the 71720 are also available as a PCIe half-length board (Model 78720), 3U VPX (Models 52720 and 53720), AMC (Model 56720), 6U cPCI (Models 72720 and 74720 with dual density), and 3U cPCI (Model 73720).

GateXpress[®] is a sophisticated configuration manager for loading and reloading the Virtex-7 FPGA. More information is available in the next page.

Products

GateXpress for FPGA-PCIe Configuration Management



The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

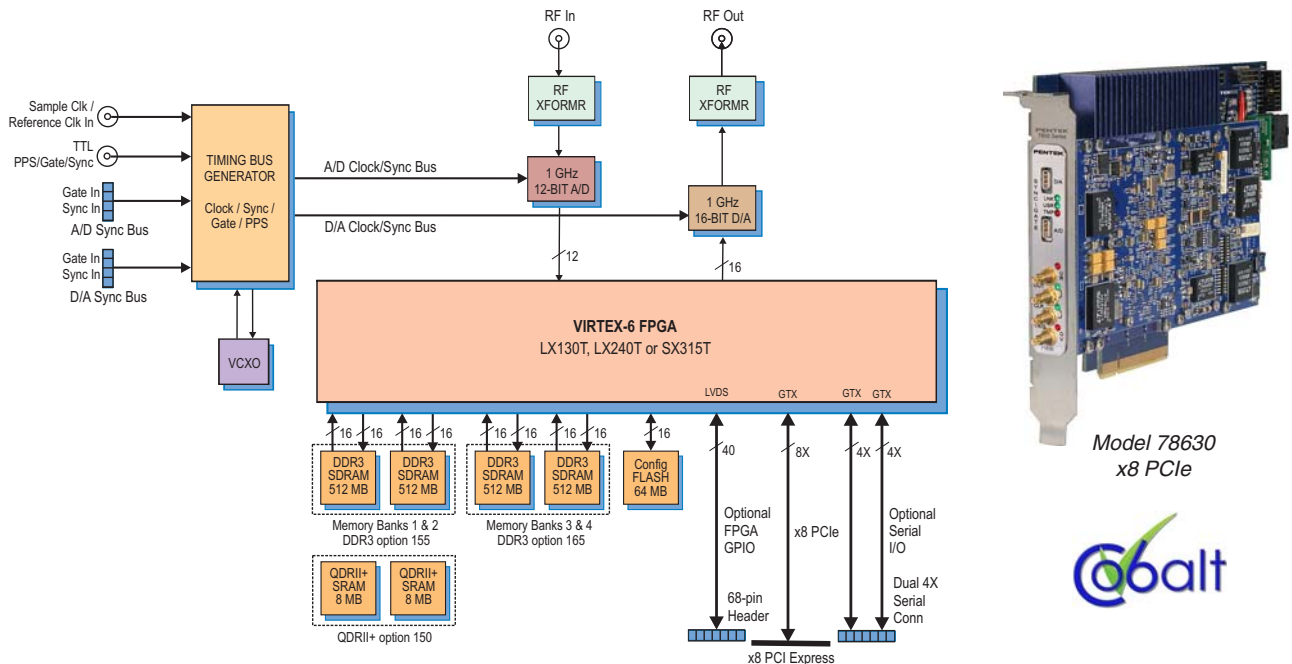
The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Products

1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA

**Model 78630 PCIe • Model 71630 XMC • Model 52630 3U VPX • Model 53630 3U VPX
Model 56630 AMC • Model 72630 6U cPCI • Model 73630 3U cPCI • Model 74630 6U cPCI**



Model 78630
x8 PCIe



Figure 55

Model 78630 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application-specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

A pair of front panel μ Sync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 78630 are also available as an XMC module (Model 71630), 3U VPX (Models 52630 and 53630), AMC (Model 56630), 6U cPCI (Models 72630 and 74630 with dual density), and 3U cPCI (Model 73630).

Products

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA

**Model 72640 6U cPCI • Model 73640 3U cPCI • Model 74640 6U cPCI
Model 71640 XMC • Model 78640 PCIe • Model 53640 3U VPX • Model 56640 AMC**

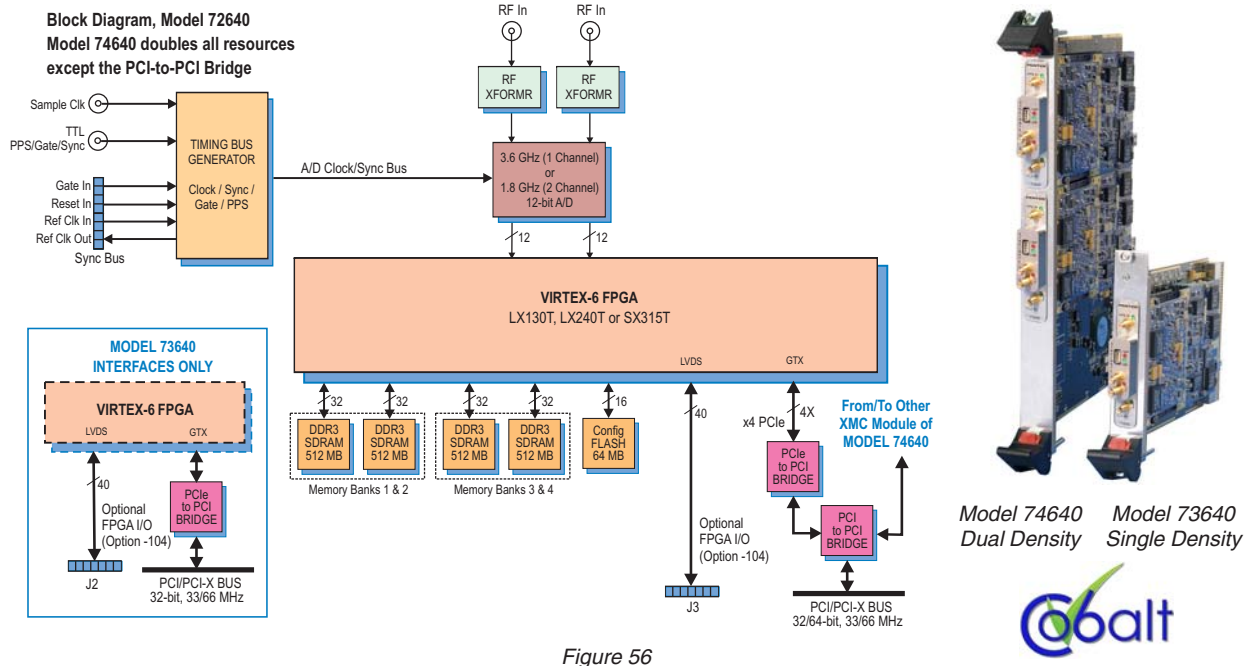


Figure 56

Models 72640, 73640 and 74640 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP

modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

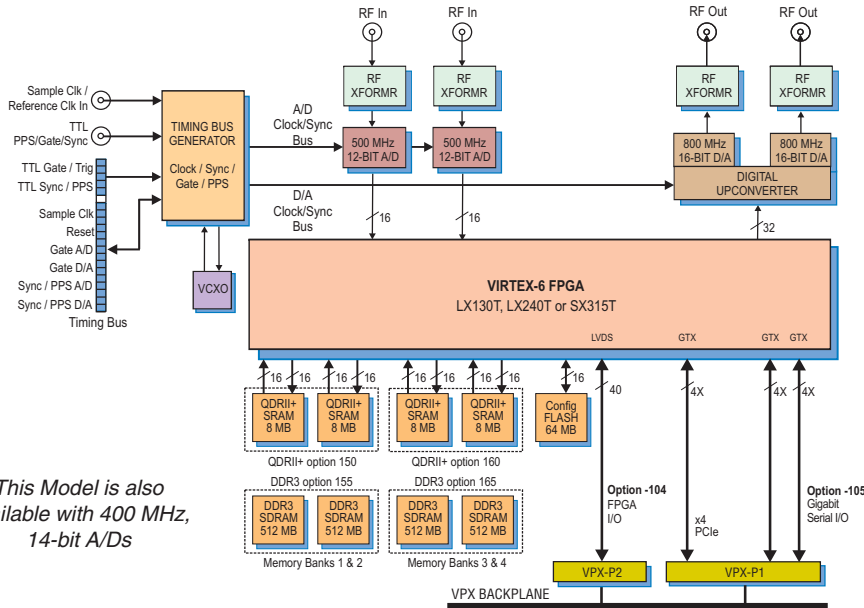
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 is a dual density 6U cPCI board. Also available is an XMC module (Model 71640), PCIe half-length board (Model 78640), 3U VPX (Models 52640 and 53640), and AMC (Model 56640).

Products

2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 52650 3U VPX • Model 53650 3U VPX • Model 71650 XMC • Model 78650 PCIe • Model 56650 AMC • Model 72650 6U cPCI • Model 73650 3U cPCI • Model 74650 6U cPCI



This Model is also available with 400 MHz, 14-bit A/Ds



Model 52650 3U VPX COTS and rugged



Figure 57

Model 52650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 52650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 52650 are also available as a 3U VPX (Model 53650), XMC module (Model 71650), as a PCIe board (Model 78650), AMC (Model 56650), 6U cPCI (Models 72650 and 74650 dual density), and 3U cPCI (Model 73650).

Products

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

**Model 71660 XMC • Model 78660 PCIe • Model 52660 3U VPX • Model 53660 3U VPX
Model 56660 AMC • Model 72660 6U cPCI • Model 73660 3U cPCI • Model 74660 6U cPCI**

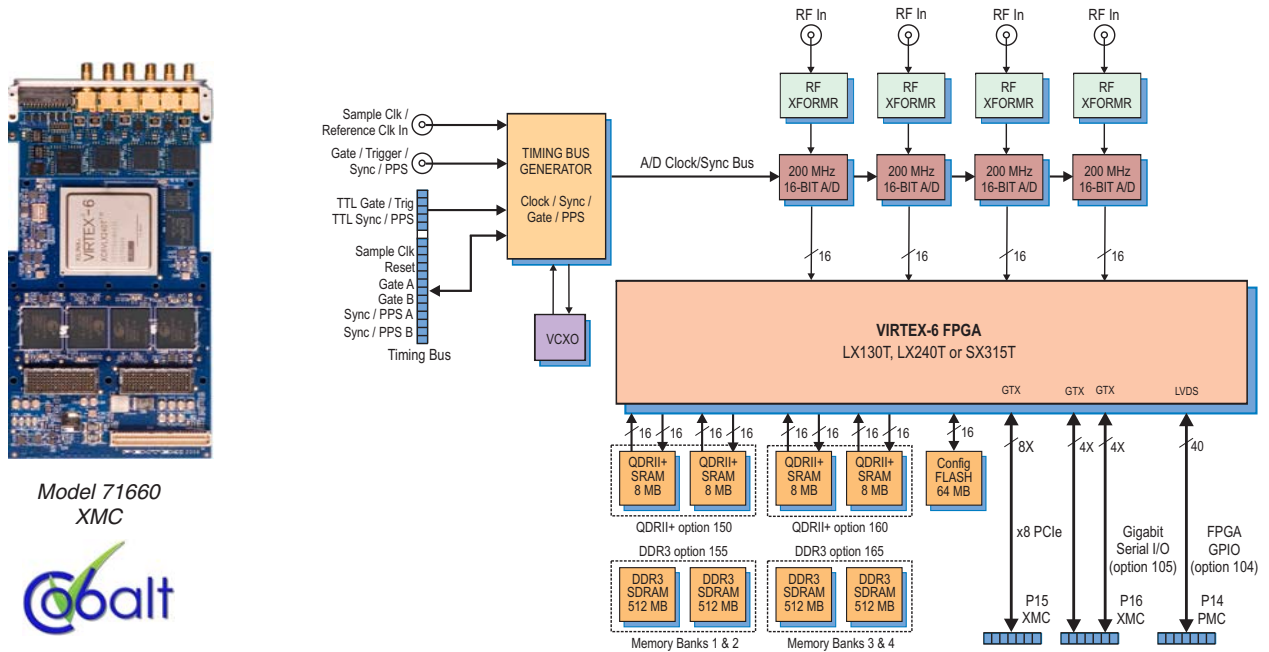


Figure 58

Model 71660 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71660 are also available as a PCIe half-length board (Model 78660), 3U VPX (Models 52660 and 53660), AMC (Model 56660), 6U cPCI (Models 72660 and 74660 with dual density), and 3U cPCI (Model 73660).

Products

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA

**Model 71760 XMC • Model 78760 PCIe • Model 52760 3U VPX • Model 53760 3U VPX
Model 56760 AMC • Model 72760 6U cPCI • Model 73760 3U cPCI • Model 74760 6U cPCI**



Model 71760
XMC

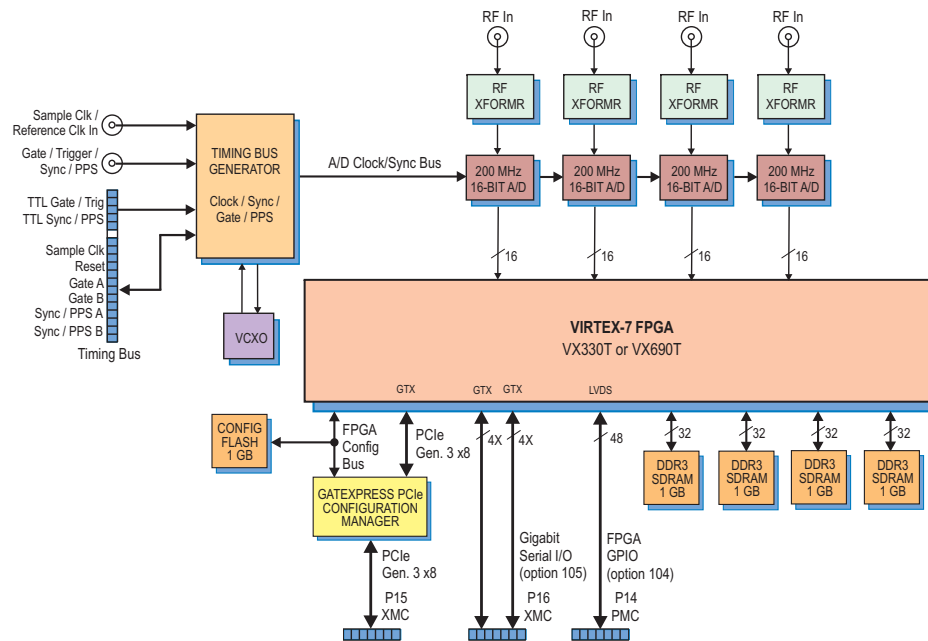


Figure 59

Model 71760 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 71760 are also available as a PCIe half-length board (Model 78760), 3U VPX (Models 52760 and 53760), AMC (Model 56760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).

Please go to page 39 for information about GateXpress.

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 71661 XMC • Model 78661 PCIe • Model 52661 3U VPX • Model 53661 3U VPX
 Model 56661 AMC • Model 72661 6U cPCI • Model 73661 3U cPCI • Model 74661 6U cPCI

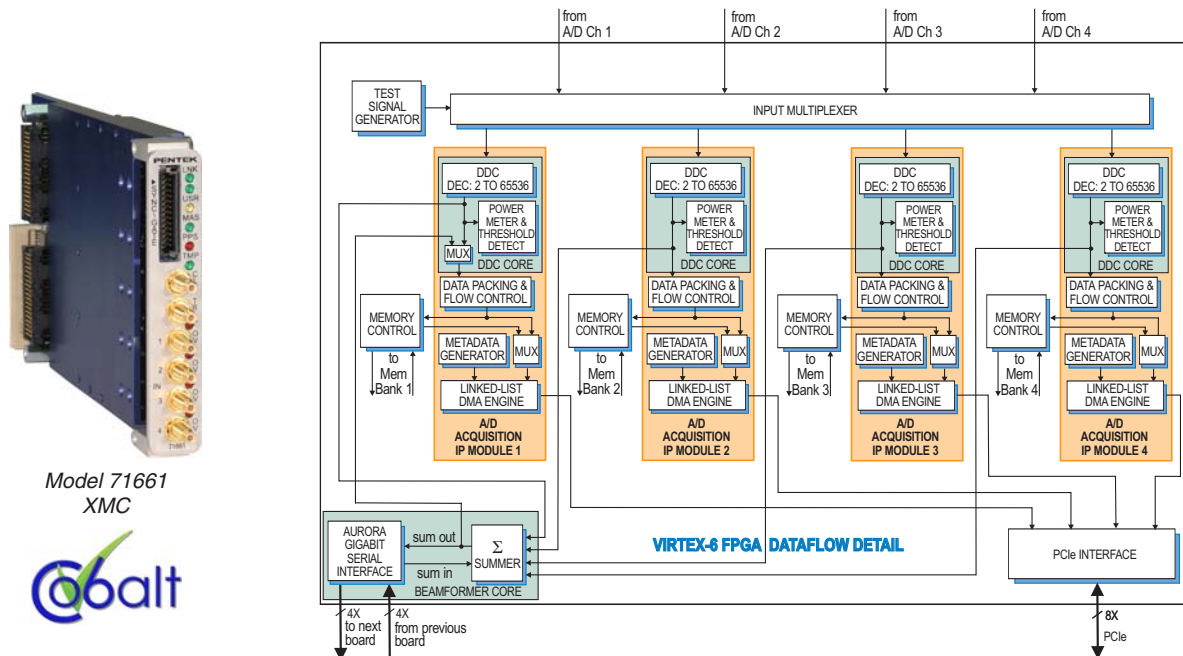


Figure 60

Model 71661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDR II+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decima-

tions can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71661 also features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

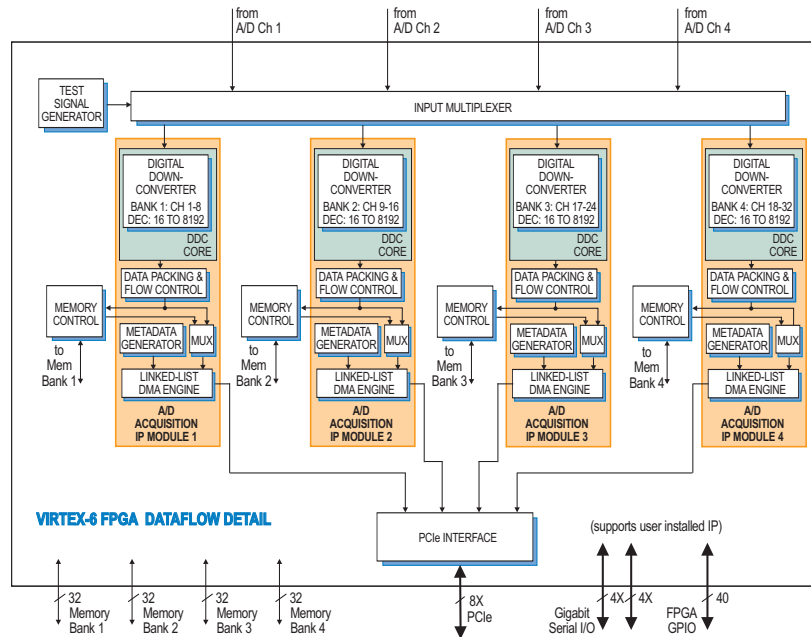
For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the 71661 are also available as a PCIe half-length board (Model 78661), 3U VPX (Models 52661 and 53661), AMC (Model 56661), 6U cPCI (Models 72661 and 74661 with dual density), and 3U cPCI (Model 73661).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 78662 PCIe • Model 71662 XMC • Model 52662 3U VPX • Model 53662 3U VPX
 Model 56662 AMC • Model 72662 6U cPCI • Model 73662 3U cPCI • Model 74662 6U cPCI



Model 78662
x8 PCIe



Figure 61

Model 78662 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192 programmable in steps

of eight. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

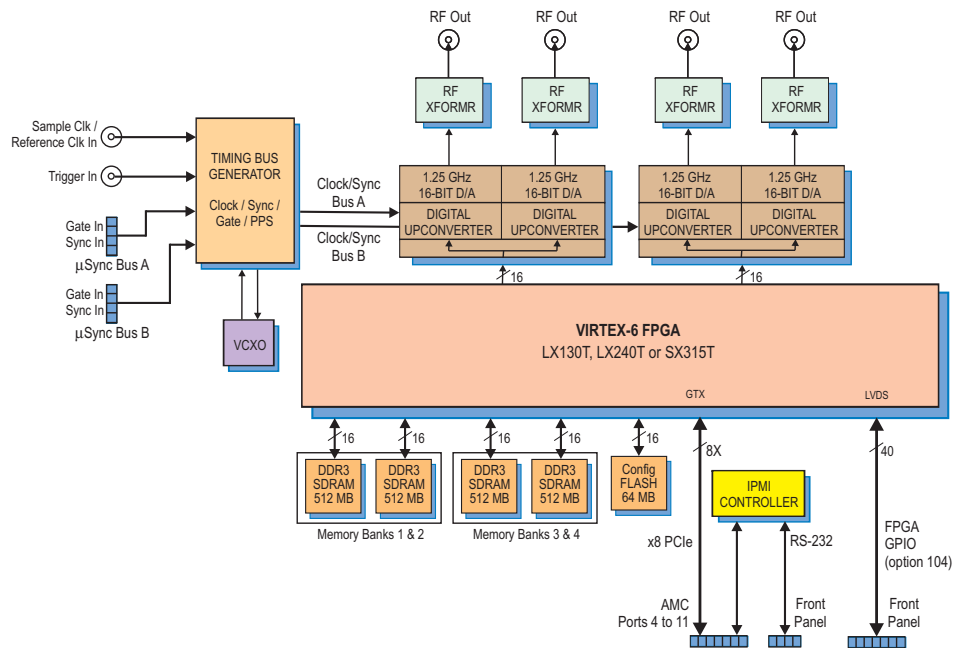
Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 78662 are also available as an XMC module (Model 71662), 3U VPX (Models 52662 & 53662), AMC (Model 56662), 6U cPCI (Models 72662 and 74662 with dual density), and 3U cPCI (Model 73662).

Products

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA

**Model 56670 AMC • Model 71670 XMC • Model 78670 PCIe • Model 52670 3U VPX
 Model 53670 3U VPX • Model 72670 6U cPCI • Model 73670 3U cPCI • Model 74670 6U cPCI**



Model 56670
AMC



Figure 62

Model 56670 is a member of the Cobalt family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

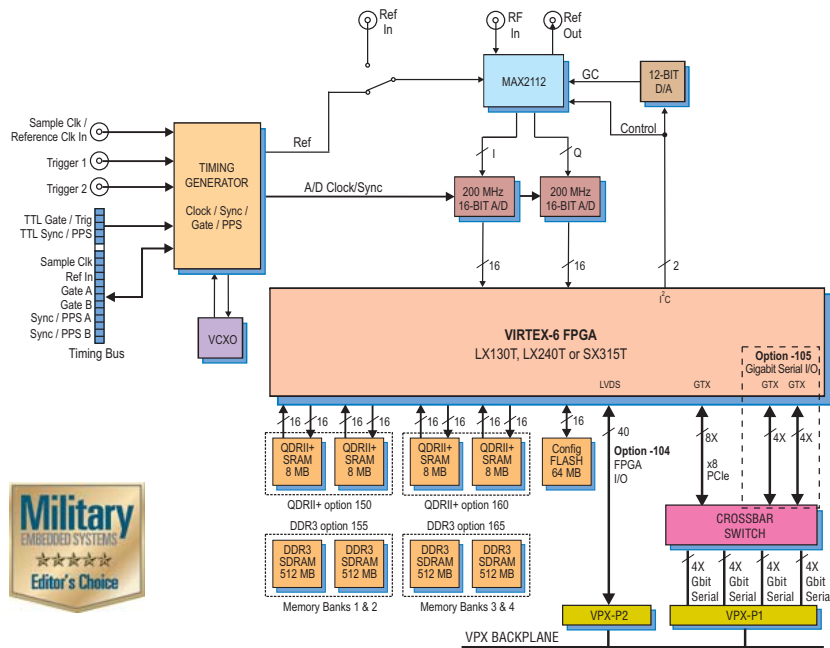
The Model 56670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Versions of the 56670 are available as an XMC (Model 71670), PCIe half-length board (Model 78670), 3U VPX (Models 52670 and 53670), 6U cPCI (Models 72670 and 74670 dual density), and 3U cPCI (Model 73670).

Products

L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA

**Model 53690 3U VPX • Model 52690 3U VPX • Model 71690 XMC • Model 78690 PCIe
Model 56690 AMC • Model 72690 6U cPCI • Model 73690 3U cPCI • Model 74690 6U cPCI**



Model 53690 3U VPX
COTS and rugged



Figure 63

Model 53690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the

board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the 53690 are also available as a 3U VPX (Model 52690), an XMC (Model 71690), as a PCIe (Model 78690), AMC (Model 56690), 6U cPCI (Models 72690 and 74690 with dual density), and 3U cPCI (Model 73690).

Products

LVDS Digital I/O with Virtex-6 FPGA

**Model 71610 XMC • Model 78610 PCIe • Model 52610 3U VPX • Model 53610 3U VPX
 Model 56610 AMC • Model 72610 6U cPCI • Model 73610 3U cPCI • Model 74610 6U cPCI**

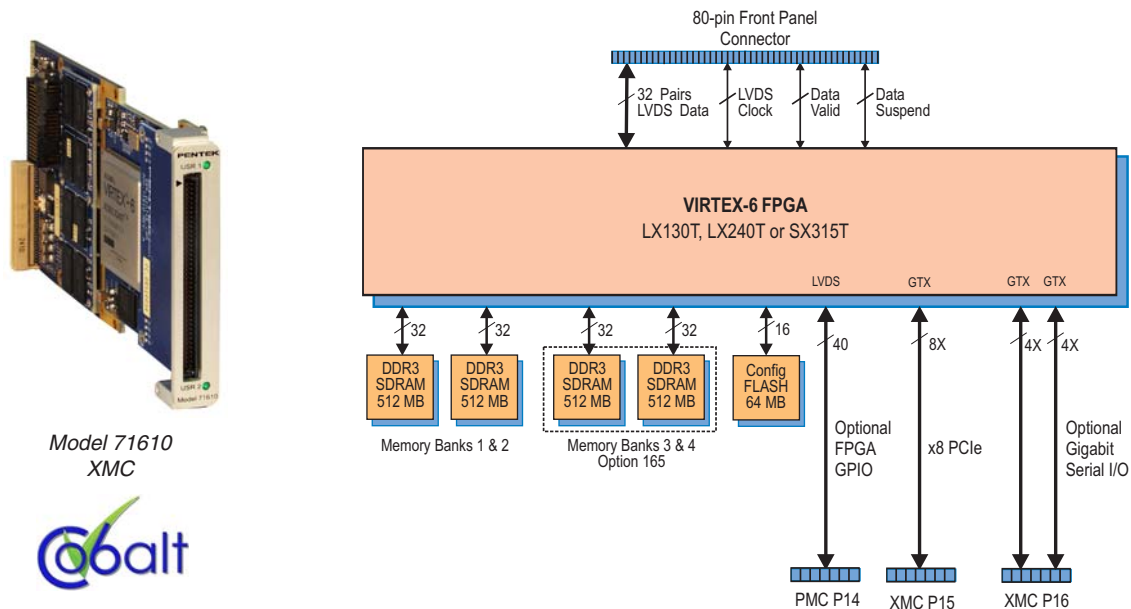


Figure 64

Model 71610 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

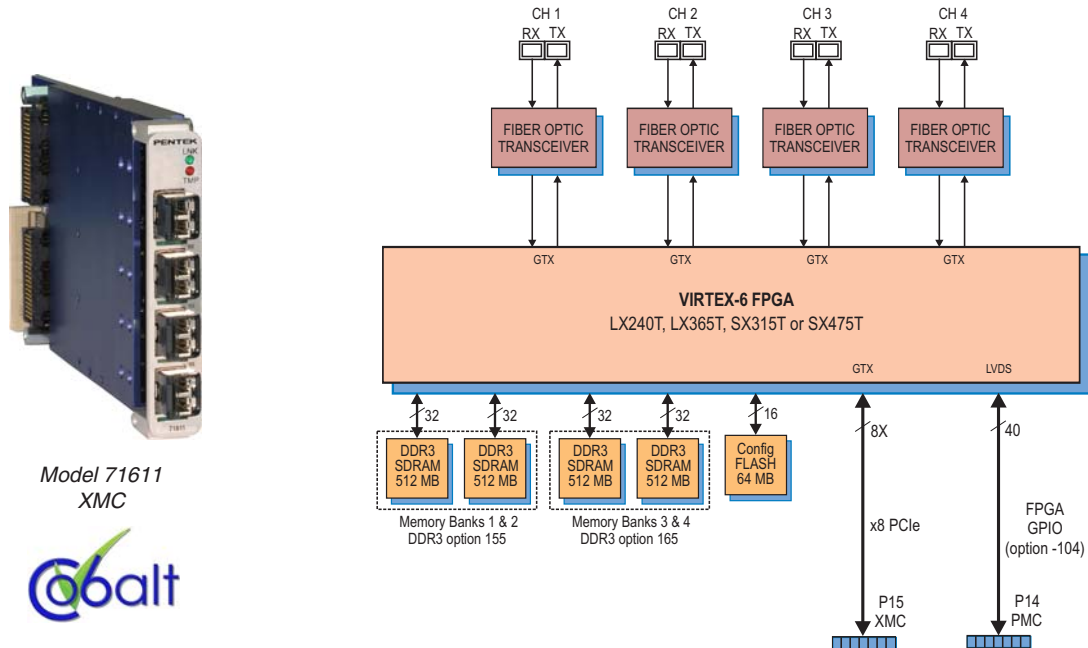
The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Versions of the 71610 are also available as a PCIe board (Model 78610), 3U VPX (Models 52610 and 53610), AMC (Model 56610), 6U cPCI (Models 72610 and 74610 with dual density), and 3U cPCI (Model 73610).

Products

Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA

**Model 71611 XMC • Model 78611 PCIe • Model 53611 3U VPX • Model 53611 3U VPX
Model 56611 AMC • Model 72611 6U cPCI • Model 73611 3U cPCI • Model 74611 6U cPCI**



Model 71611
XMC



Figure 65

Model 71611 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, gigabit serial interface, it is ideal for interfacing to serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container

for data processing applications where each function exists as an intellectual property (IP) module.

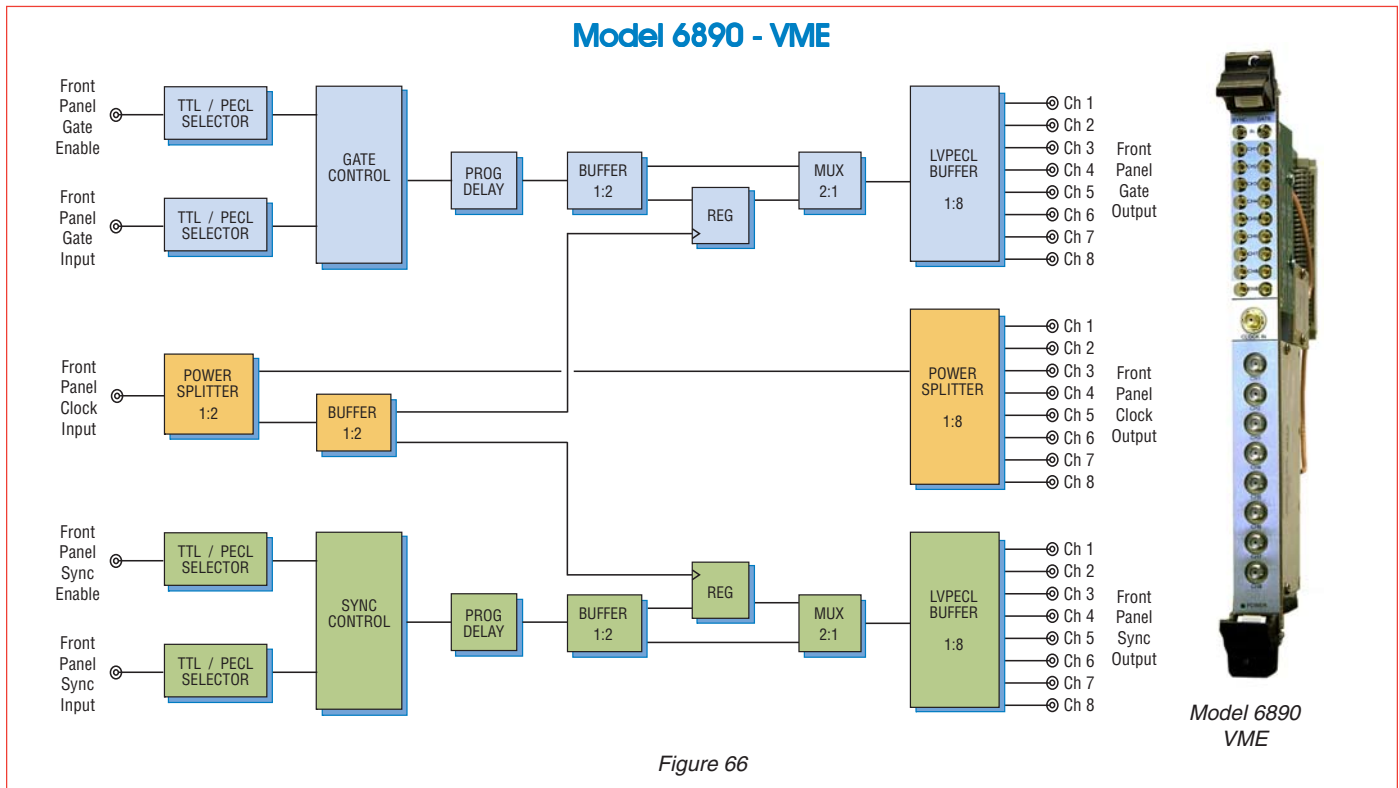
IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 71611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop.

Versions of the 71611 are also available as a PCIe board (Model 78611), 3U VPX (Models 52611 and 53611), AMC (Model 56611), 6U cPCI (Models 72611 and 74611 with dual density), and 3U cPCI (Model 73611).

Products

2.2 GHz Clock, Sync and Gate Distribution Board



Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power

splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

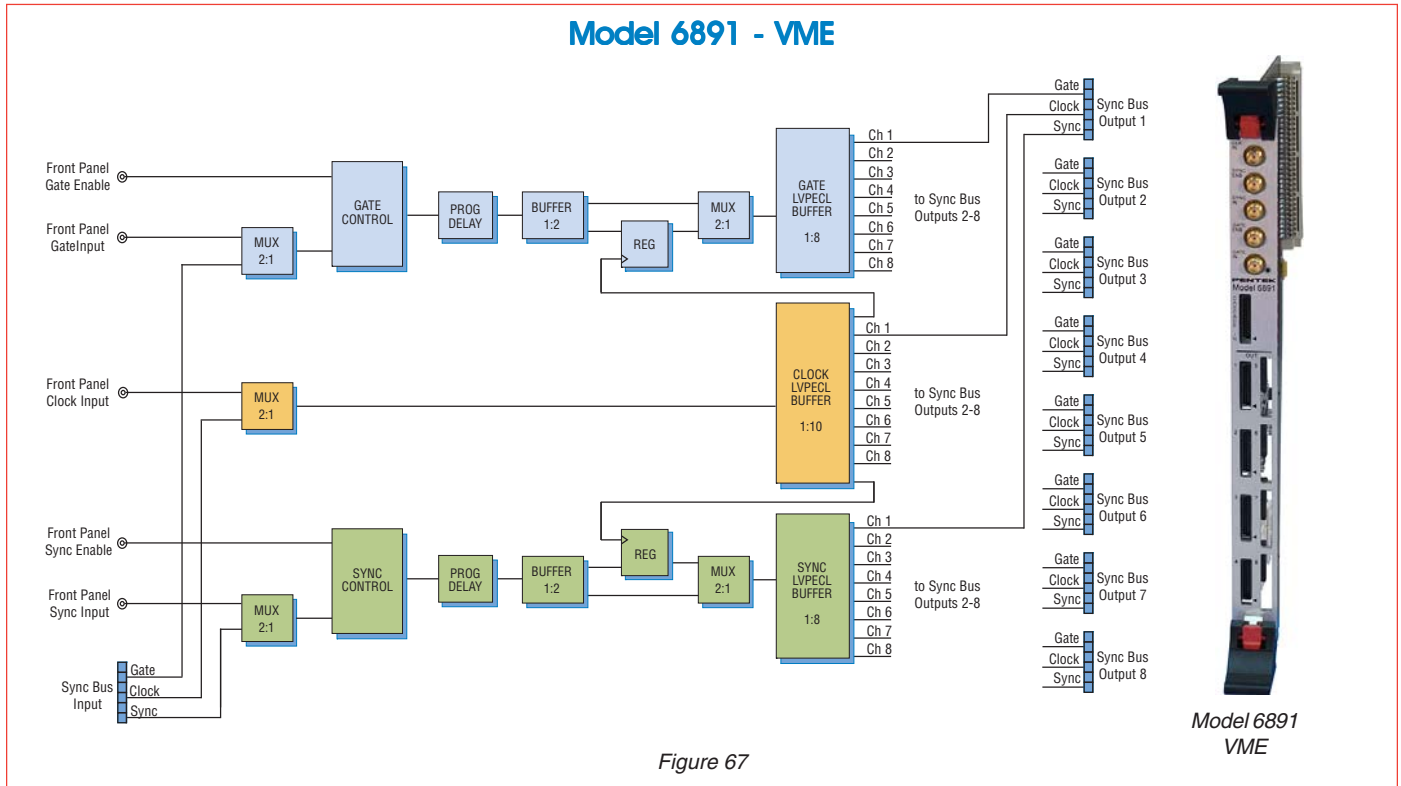
A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.

Products

System Synchronizer and Distribution Board



Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Products

Multifrequency Clock Synthesizer

**Model 7190 PMC • Model 7290 6U cPCI • Model 7390 3U cPCI • Model 7690 PCI
 Model 7790 Full-length PCIe • Model 7890 Half-length PCIe • Model 5390 3U VPX**

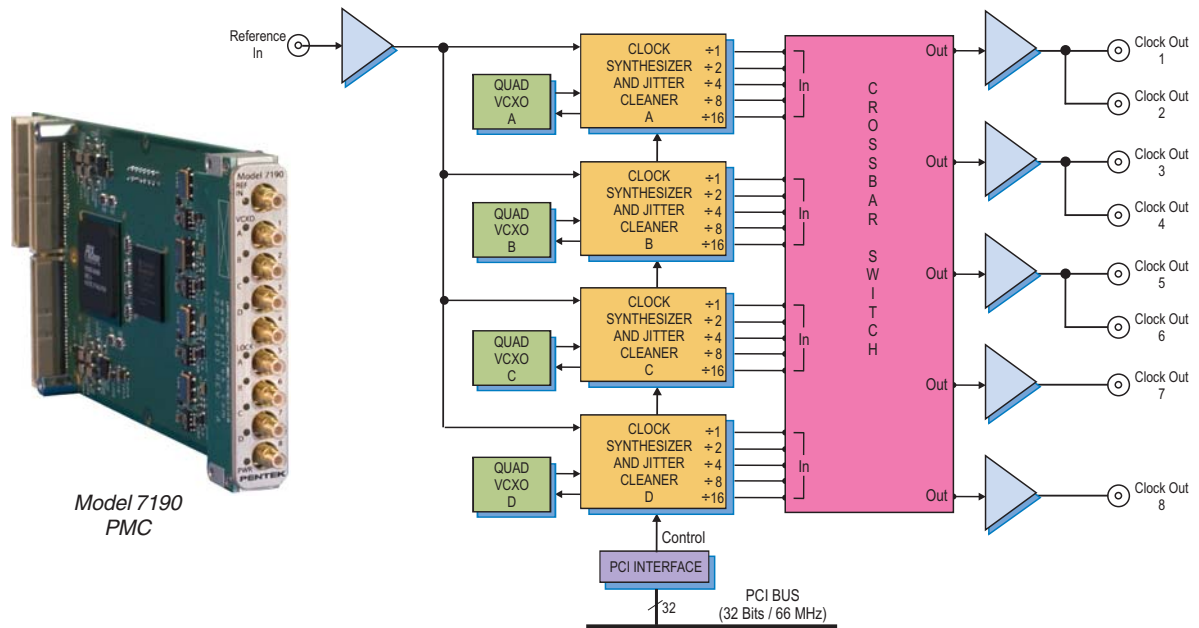


Figure 68

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs and can be phase-locked to an external reference signal.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 MHz and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7190 are also available as a PCIe full-length board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), 3U VPX board (Model 5390), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).

Products

Programmable Multifrequency Clock Synthesizer

**Model 7191 PMC • Model 7291 6U cPCI • Model 7391 3U cPCI • Model 7691 PCI
 Model 7791 Full-length PCIe • Model 7891 Half-length PCIe • Model 5391 3U VPX**

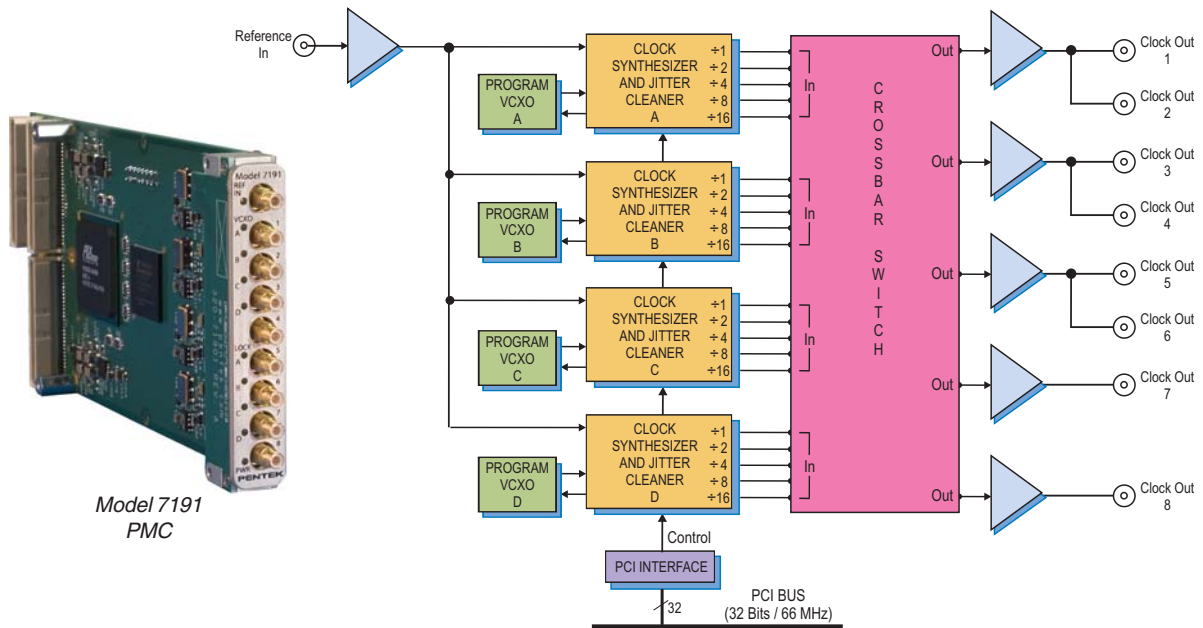


Figure 69

Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

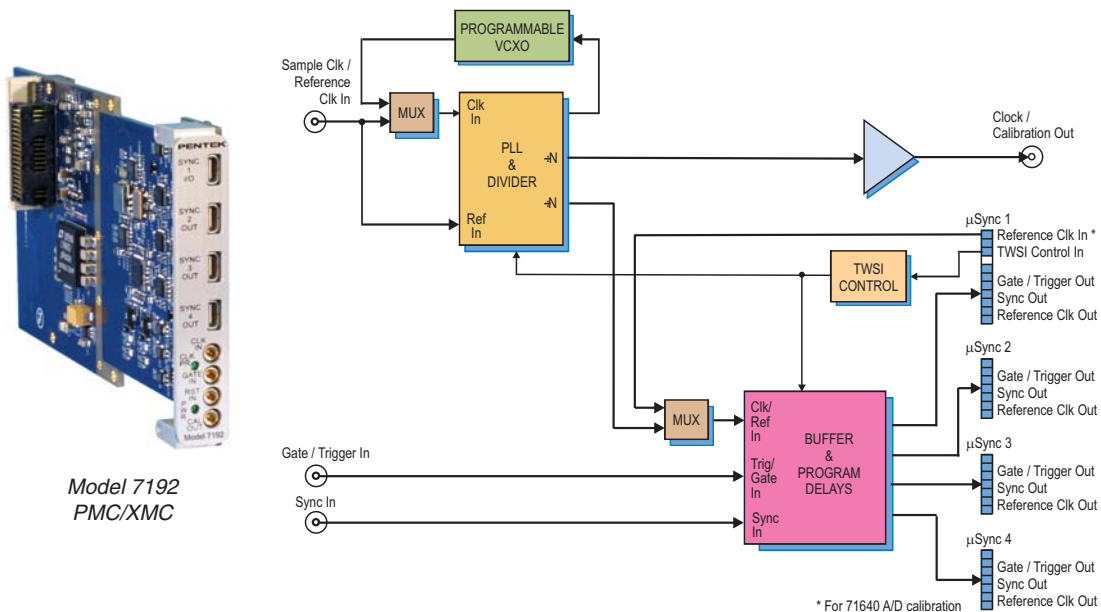
Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7191 are also available as a PCIe full-length board (Models 7791 and 7791D dual density), PCIe half-length board (Model 7891), 3U VPX board (Model 5391), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).

Products

High-Speed Synchronizer and Distribution Board

**Model 7192 PMC/XMC • Model 7892 Half-length PCIe • Model 5293 3U VPX
Model 7292 6U cPCI • Model 7392 3U cPCI • Model 7492 6U cPCI**



Model 7192
PMC/XMC

* For 71640 A/D calibration

Figure 70

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel μ Sync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

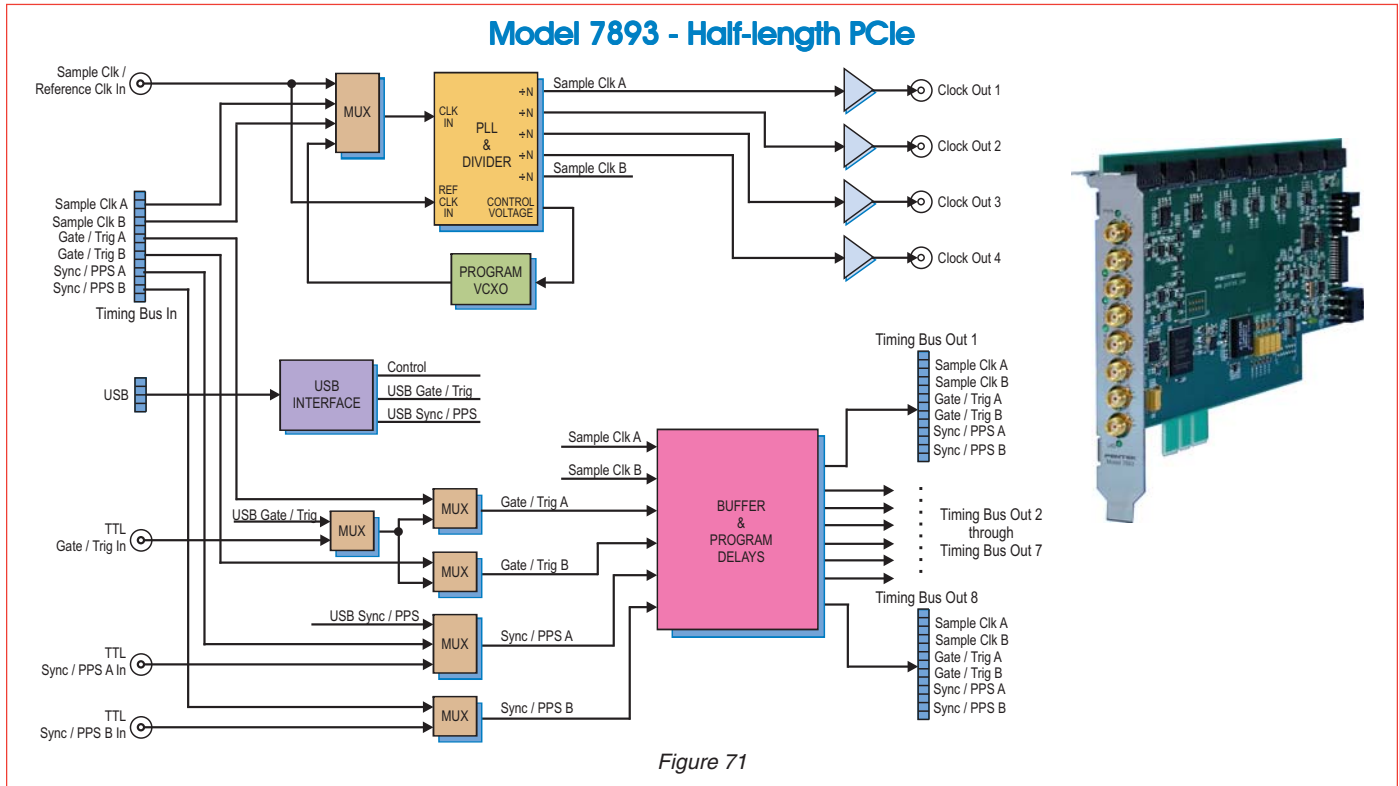
The 7192 provides four front panel μ Sync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The μ Sync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Versions of the 7192 are also available as a PCIe half-length board (Model 7892), 3U VPX (Model 5292), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).

Products

System Synchronizer and Distribution Board



Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

The Model 7893 provides four front panel SMA connectors to accept LVTTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.

Products

High-Speed Clock Generator

**Model 7194 PMC/XMC • Model 7894 Half-length PCIe • Model 5294 3U VPX
 Model 5694 AMC • Model 7294 6U cPCI • Model 7394 3U cPCI • Model 7492 6U cPCI**



Model 7194
 PMC/XMC

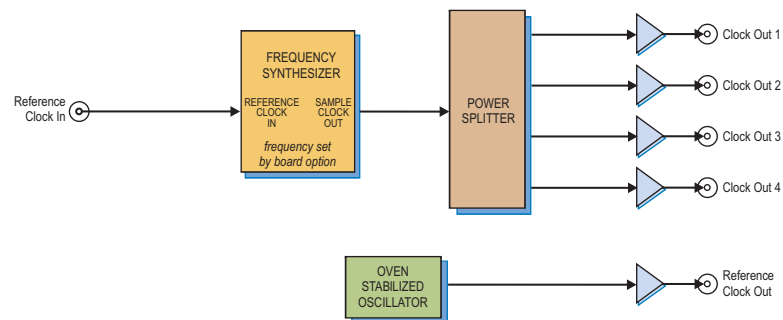


Figure 72

Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

The Model 7194 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

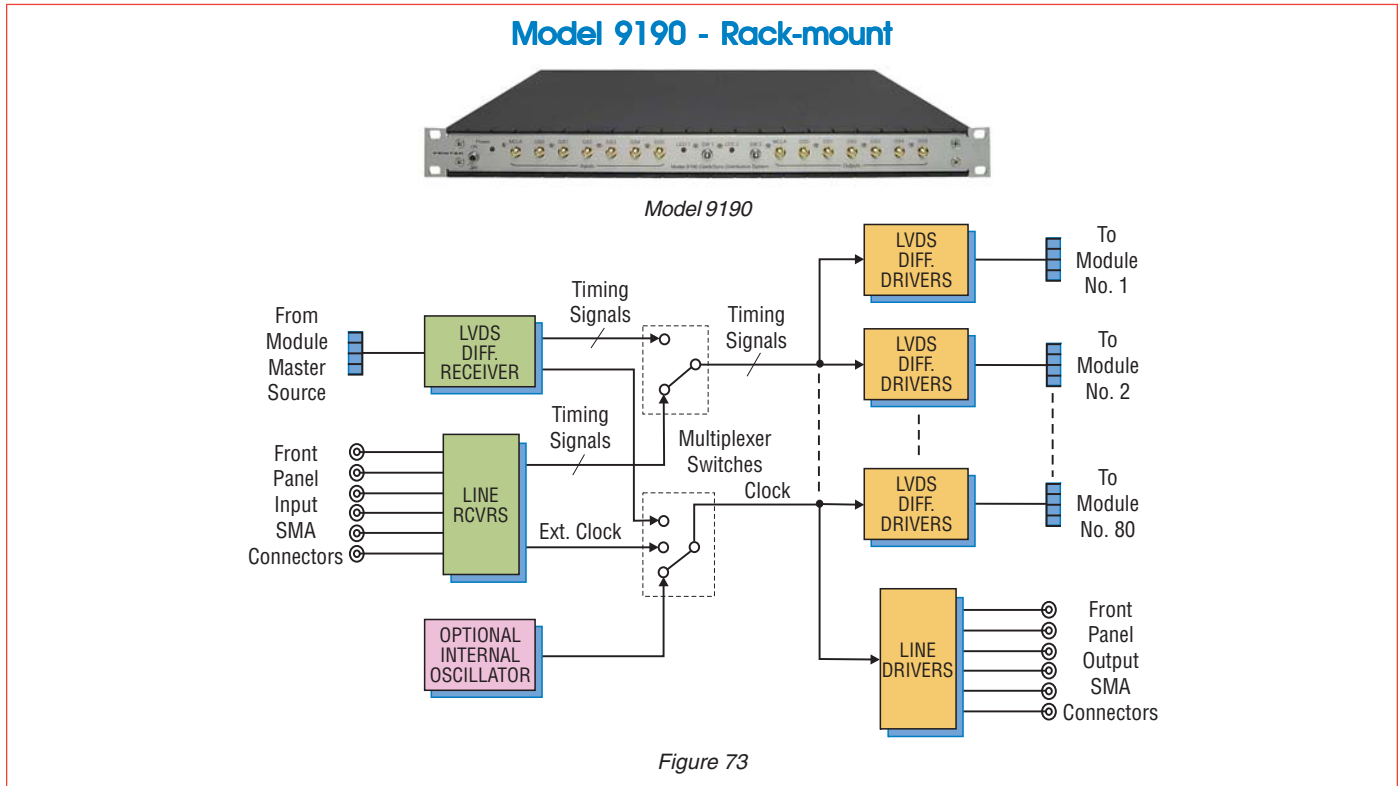
In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock. The reference is an OXCO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power. The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Versions of the 7194 are also available as a PCIe half-length board (Model 7894), 3U VPX (Model 5294), AMC (Model 5694), 6U cPCI (Models 7294 and 7494 dual density), and 3U cPCI (Model 7394).

Products

Clock and Sync Generator for I/O Modules



Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190.

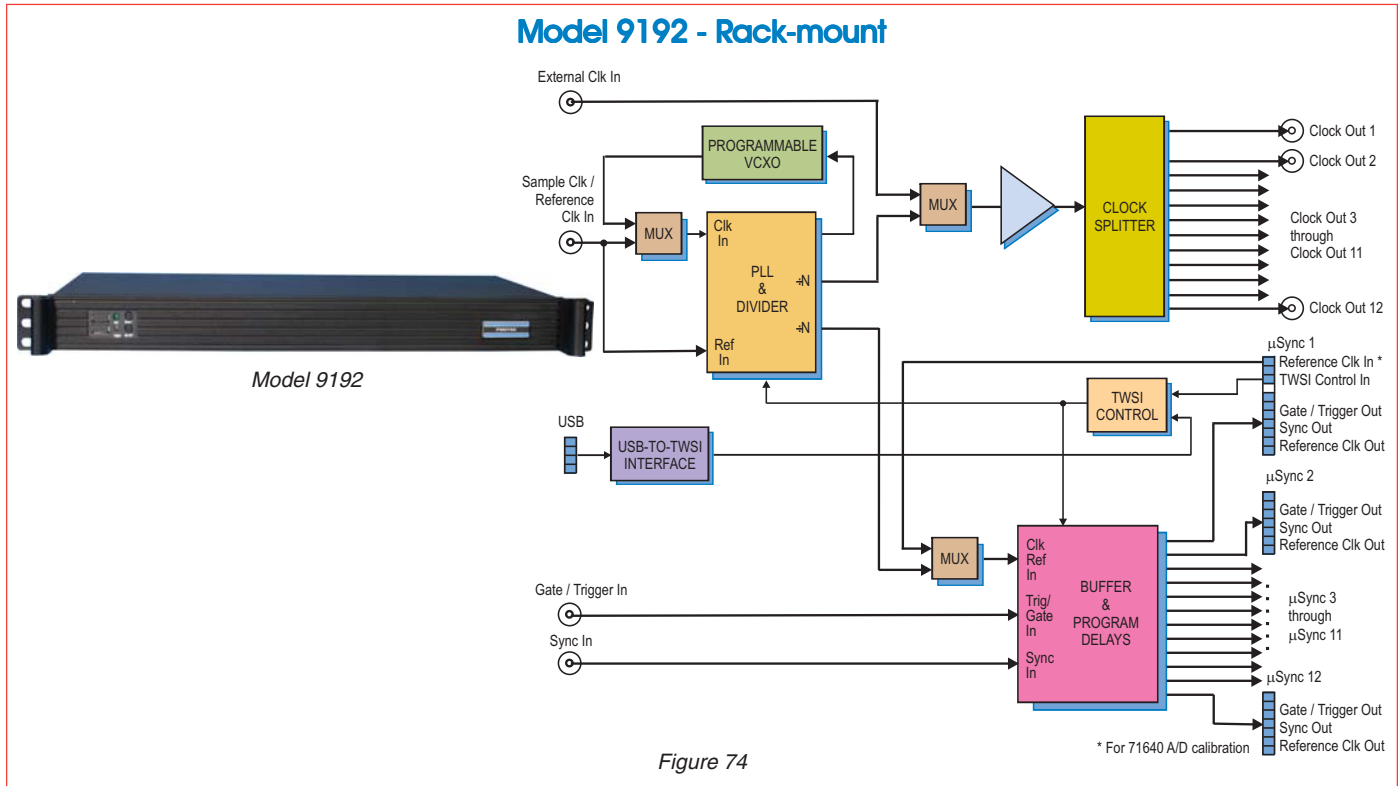
Buffered versions of the clock and five timing signals are available as outputs on the 9190's front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

Products

High-Speed System Synchronizer Unit



Model 9192 Rack-mount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel μ Sync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel μ Sync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The μ Sync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the μ Sync connectors.

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support high-speed models in the Onyx family as they become available.

Products

Eight-Channel RF/IF, 200 MS/sec Rackmount Recorder

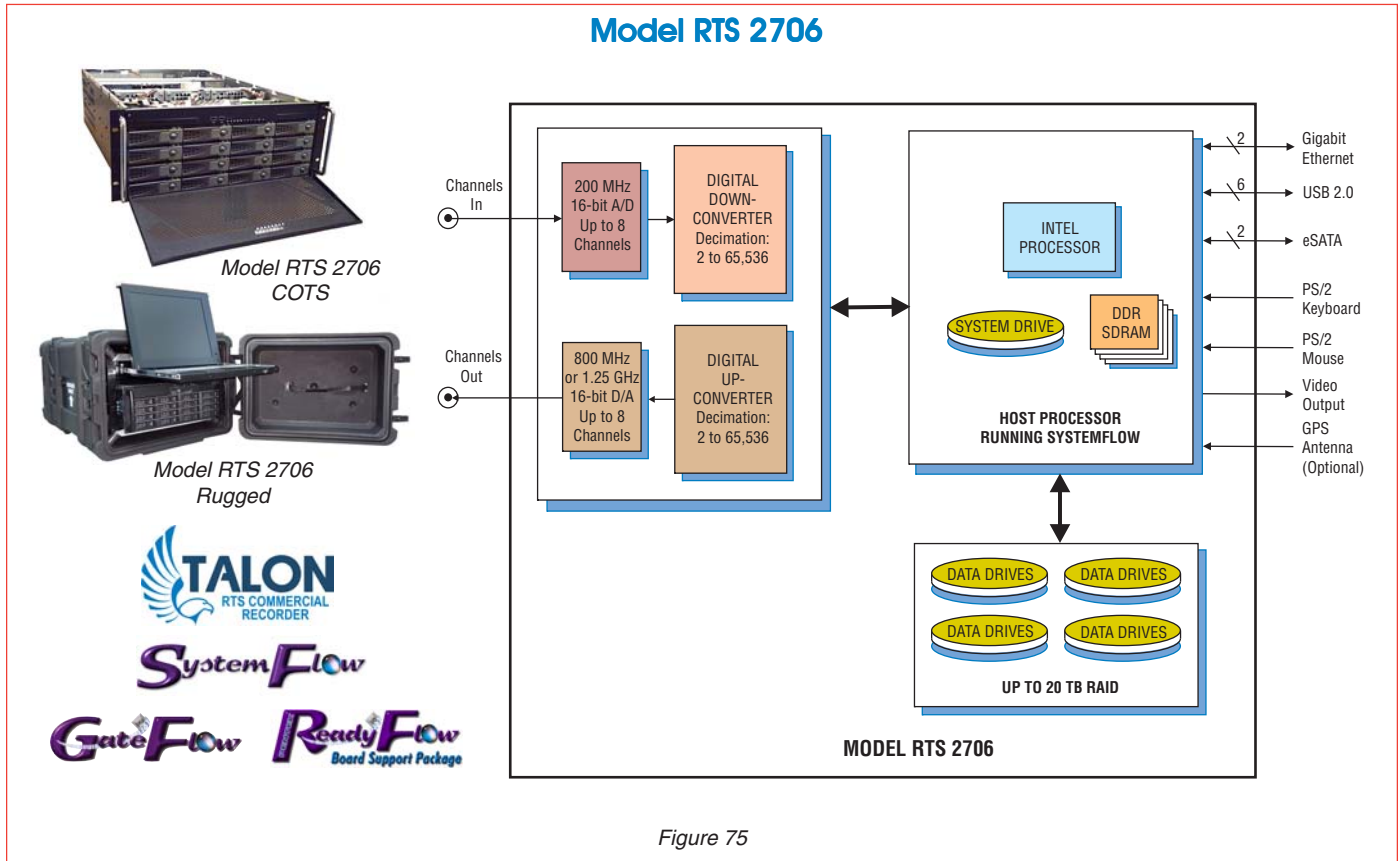


Figure 75

The Talon® RTS 2706 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2706 uses 16-bit, 200 MHz A/D converters and provides sustained recording rates up to 2.0 GB/sec in four-channel configuration.

The RTS 2706 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

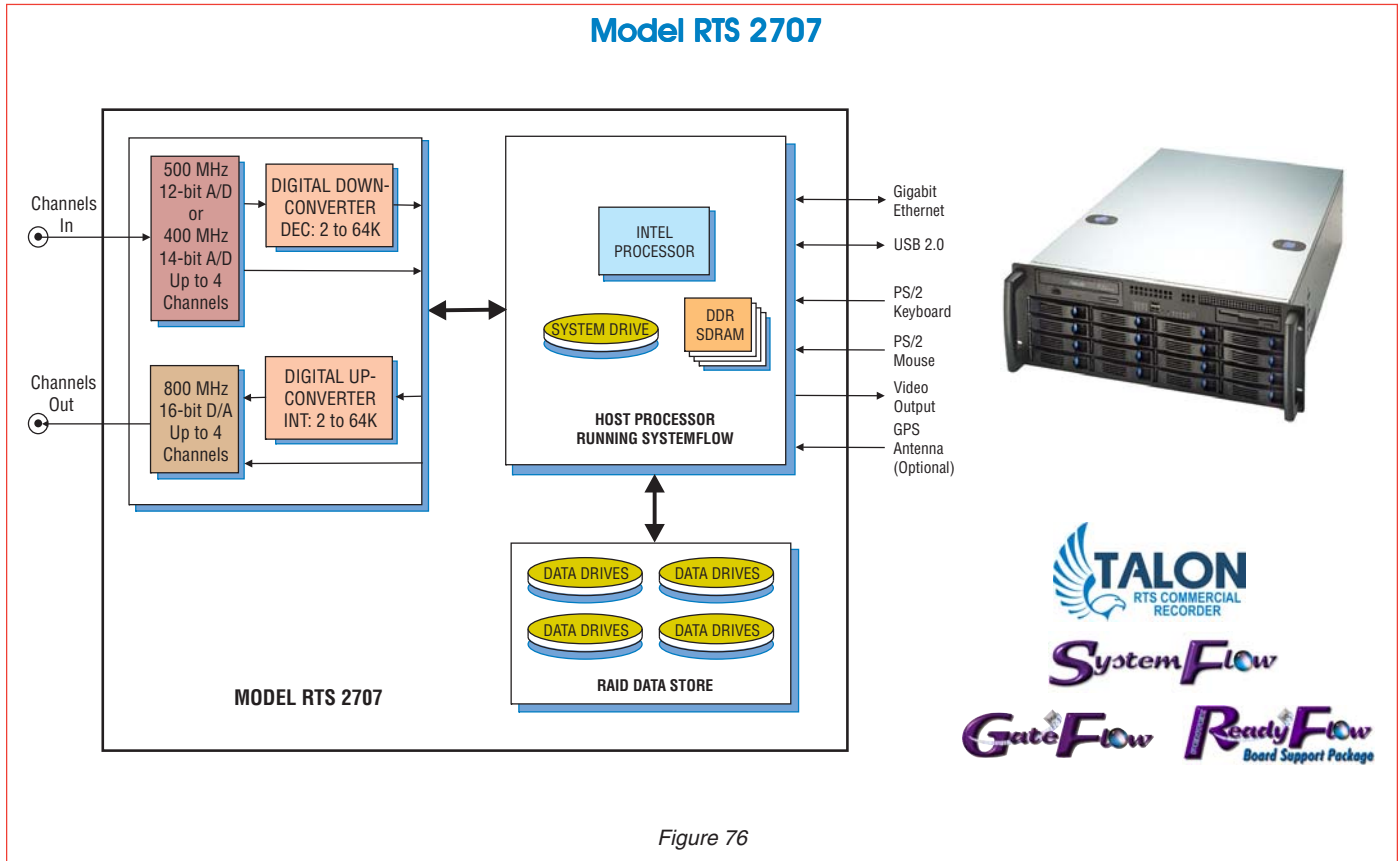
Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Built on a Windows® 7 Professional workstation with high performance Intel® Core™ i7 processor, the RTS 2706 allows the user to install post-processing and analysis tools to operate on the recorded data. The instrument records data to the native NTFS file system, providing immediate access to the data.

The RTS 2706 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Products

Four-Channel RF/IF, 500 MS/sec Rackmount Recorder



The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides sustained recording rates up to 1.6 GB/sec in two-channel configuration.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

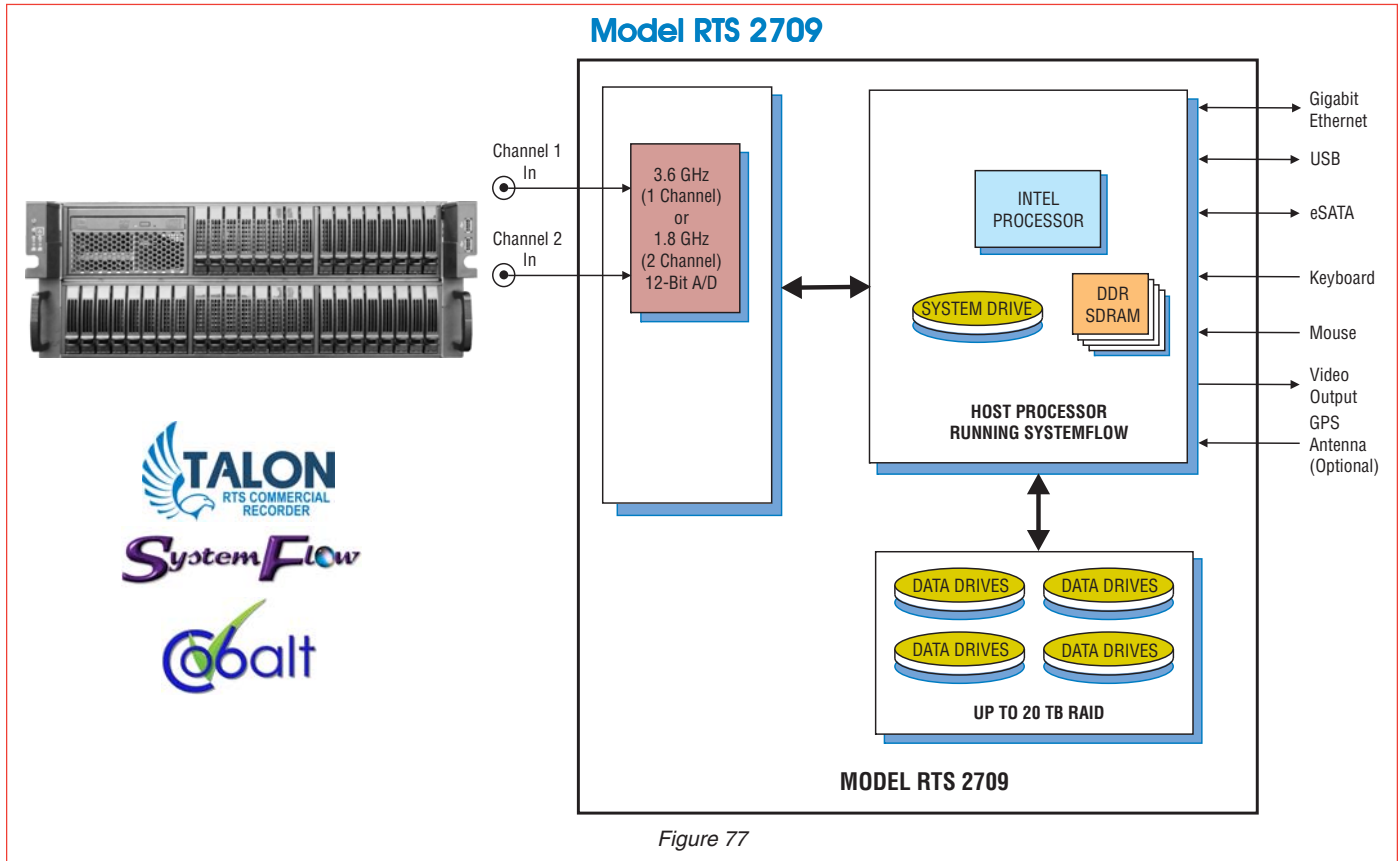
Included with the system is the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTS 2707 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2707 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2707 is configured in a 4U 19" rackmountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to increase channel counts and aggregate data rates.

Products

Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rackmount Recorder



The Talon RTS 2709 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2709 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3.2 GB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2709 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system.

Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2709 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2709 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2709 records data to the native NTFS file system that provides immediate access to the data. The RTS 2709 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Products

Two-Channel 10-Gigabit Ethernet Rackmount Recorder

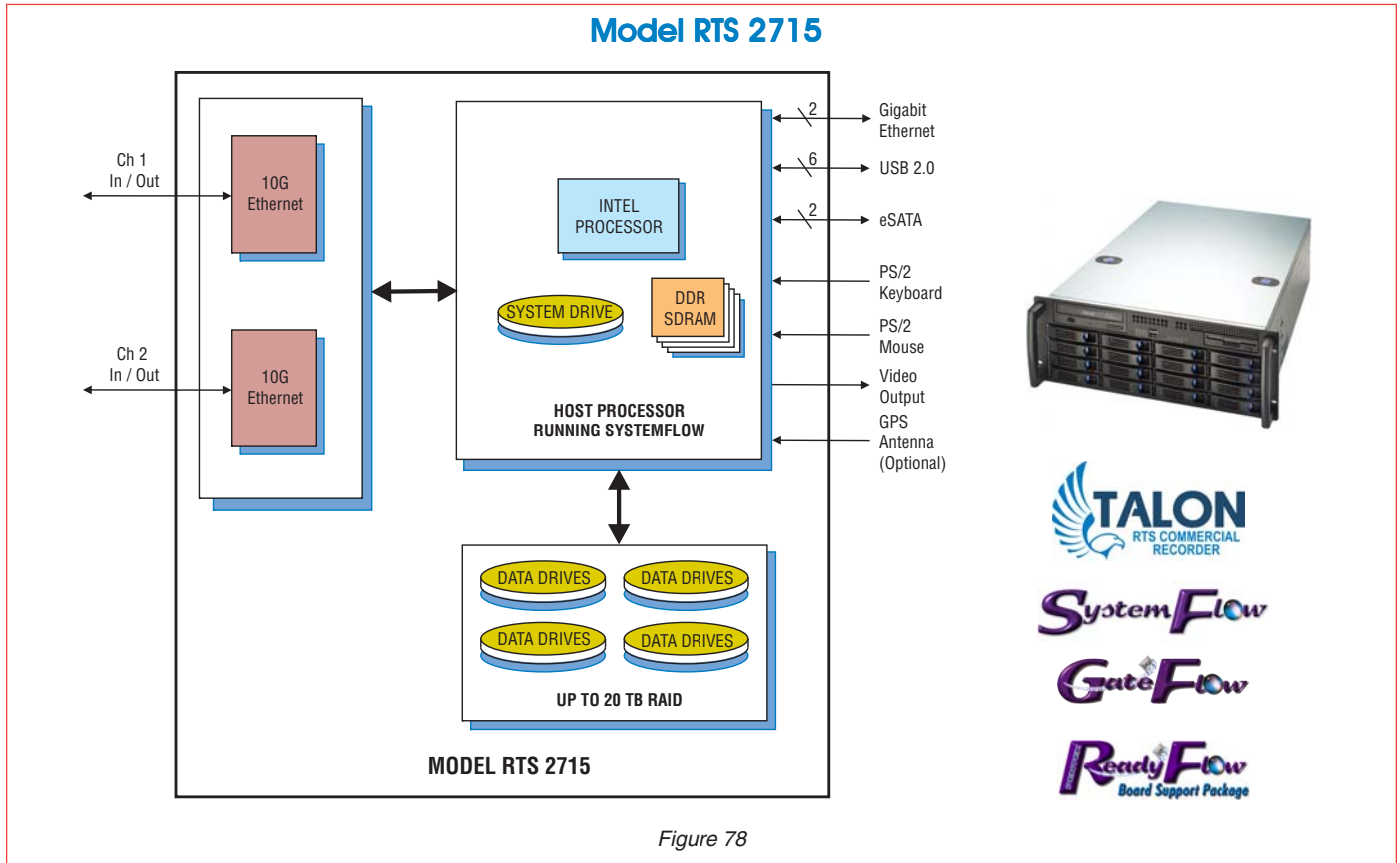


Figure 78

The Talon RTS 2715 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later

loaded as needed, allowing the user to select preconfigured settings with a single click.

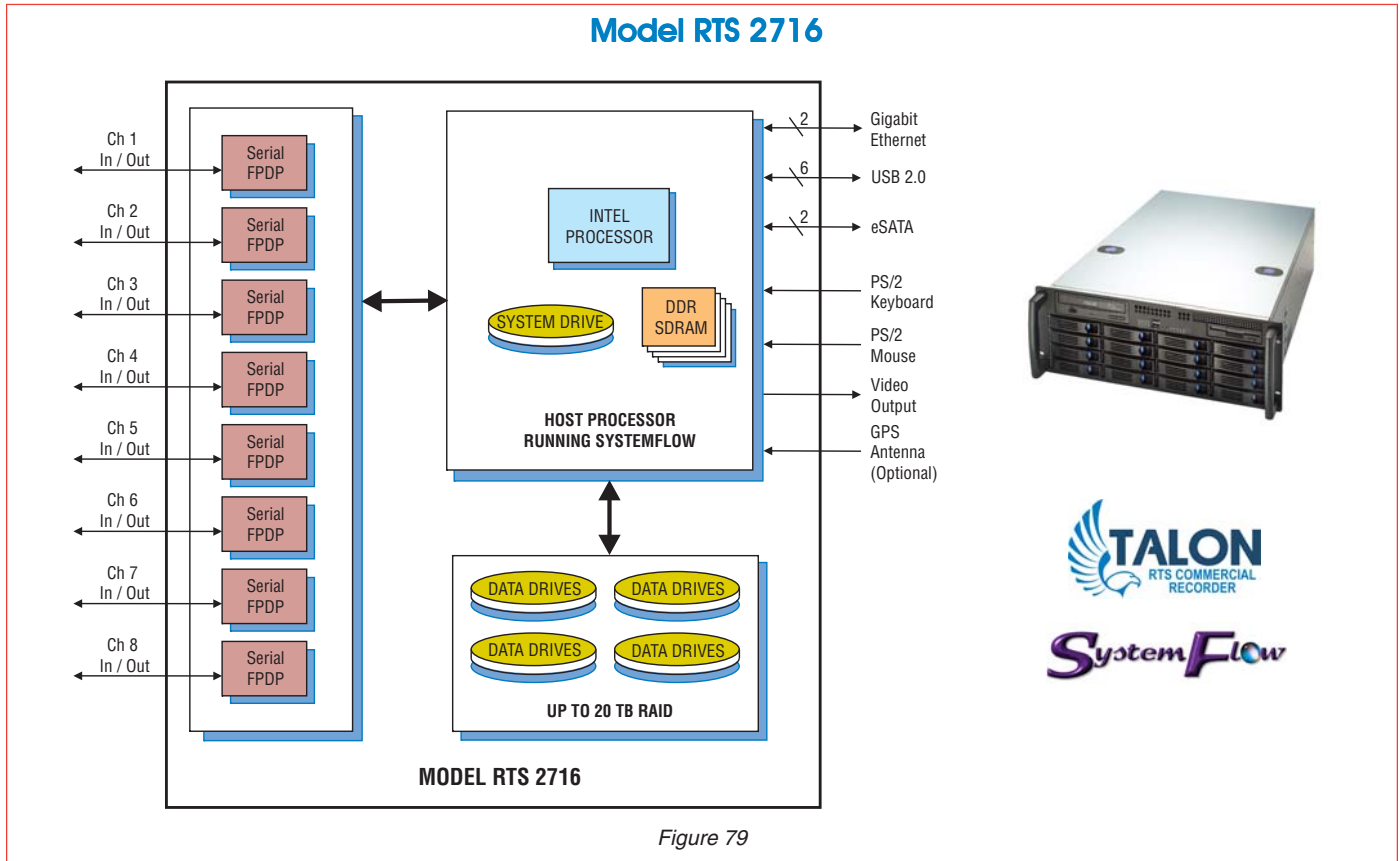
Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Products

Eight-Channel Serial FPDP Rackmount Recorder



The Talon RTS 2716 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.4 GB/sec.

The RTS 2716 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625,

2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per serial FPDP link.

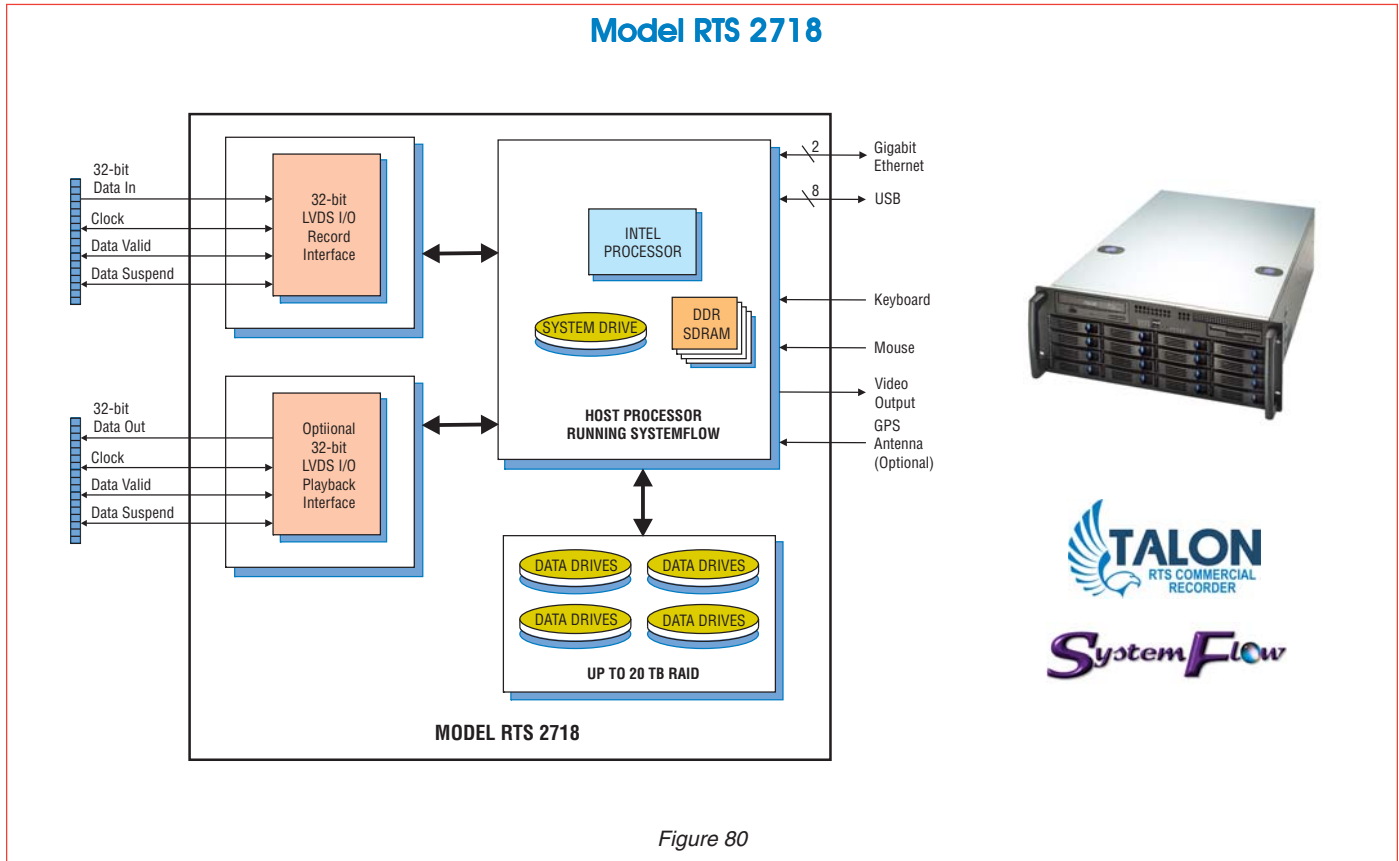
Built on a server-class Windows 7 Professional workstation, the RTS 2716 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2716 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2716 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Up to 24 hot-swappable SATA drives are optionally available, allowing up to 20 terabytes of real-time data storage space in a single chassis.

The RTS 2716 includes the SystemFlow Recording Software, which features a Windows-based GUI that provides a simple and intuitive means to configure and control the system.

Products

LVDS Digital I/O Rackmount Recorder



The Talon RTS 2718 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves sustained recording rates of up to 1 GB/sec.

The RTS 2718 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

The RTS 2718 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTS 2718 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2718 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or eight USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD \pm R/RW drive.

The RTS 2718 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Products

Four-Channel RF/IF 200 MS/sec Rugged Portable Recorder

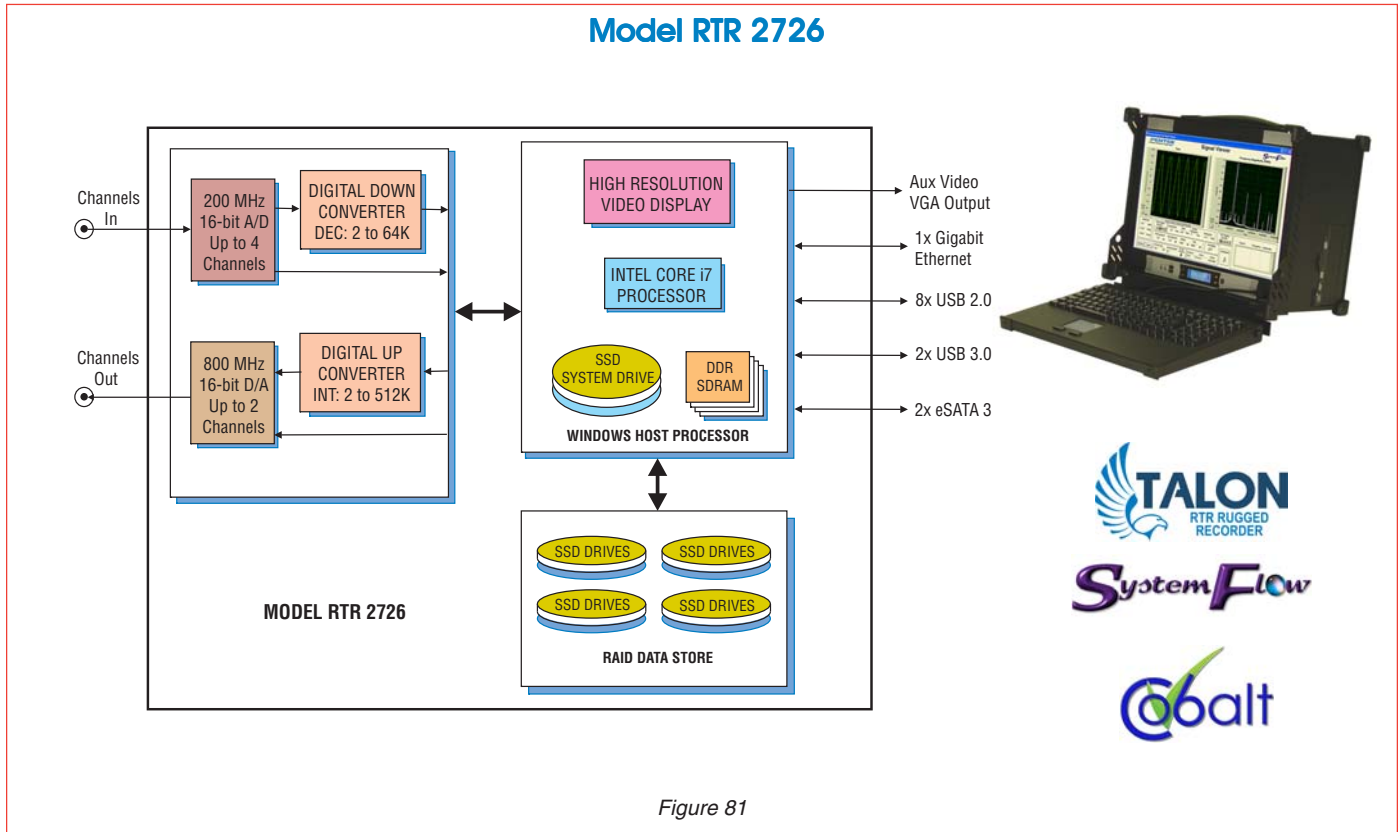


Figure 81

The Talon RTR 2726 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726 provides sustained recording rates of up to 1.6 GB/sec in a four-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726 is supplied in a small footprint portable package measuring just 16.9" W x 9.5" D x 13.4" H and weighing about 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2726 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and

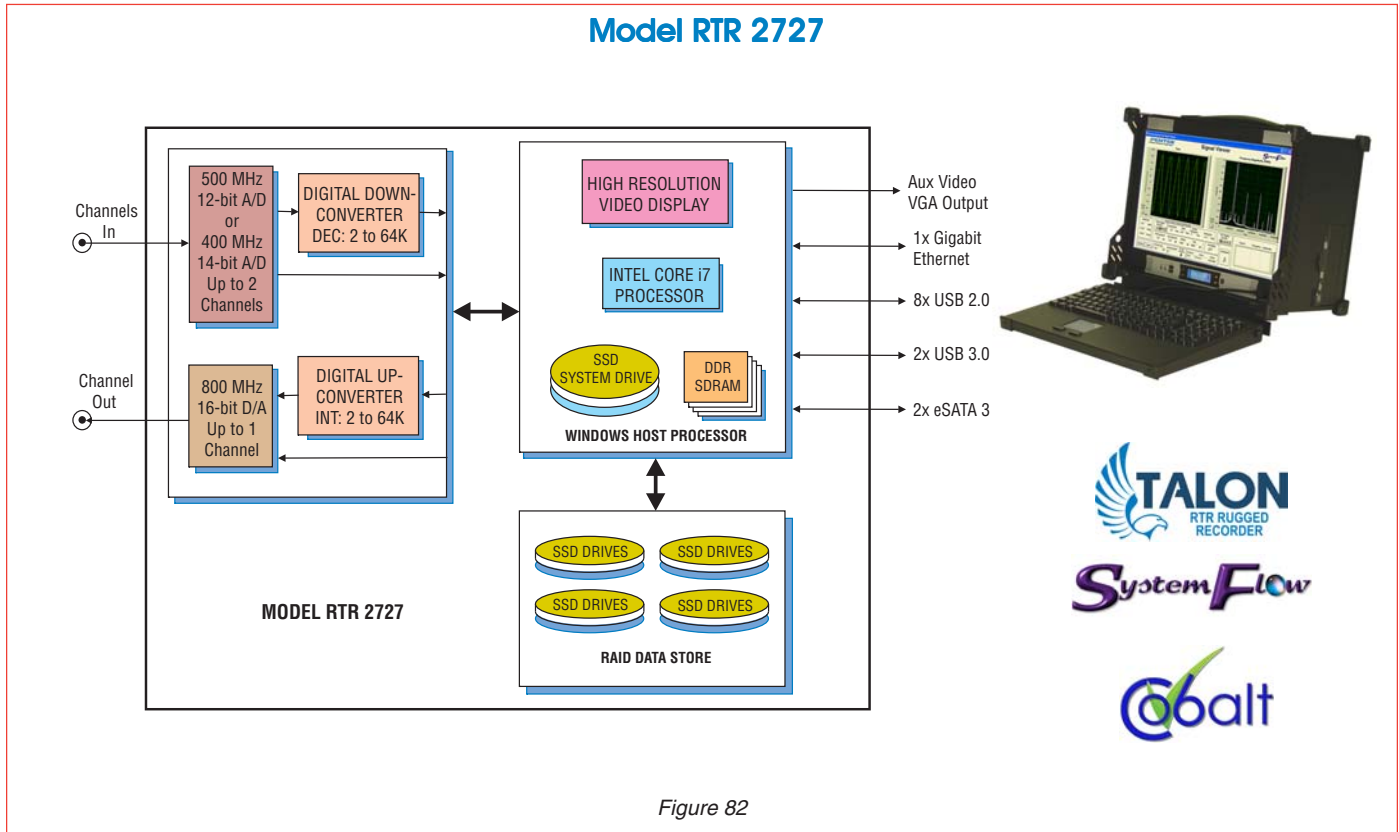
D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2726 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2726 performs well in ground, shipborne and airborne environments.

Products

Two-Channel RF/IF 500 MS/sec Rugged Portable Recorder



The Talon RTR 2727 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2727 provides sustained recording rates of up to 2.0 GB/sec in a two-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2727 is supplied in a small footprint portable package measuring just 16.9" W x 9.5" D x 13.4" H and weighing about 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2727 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and

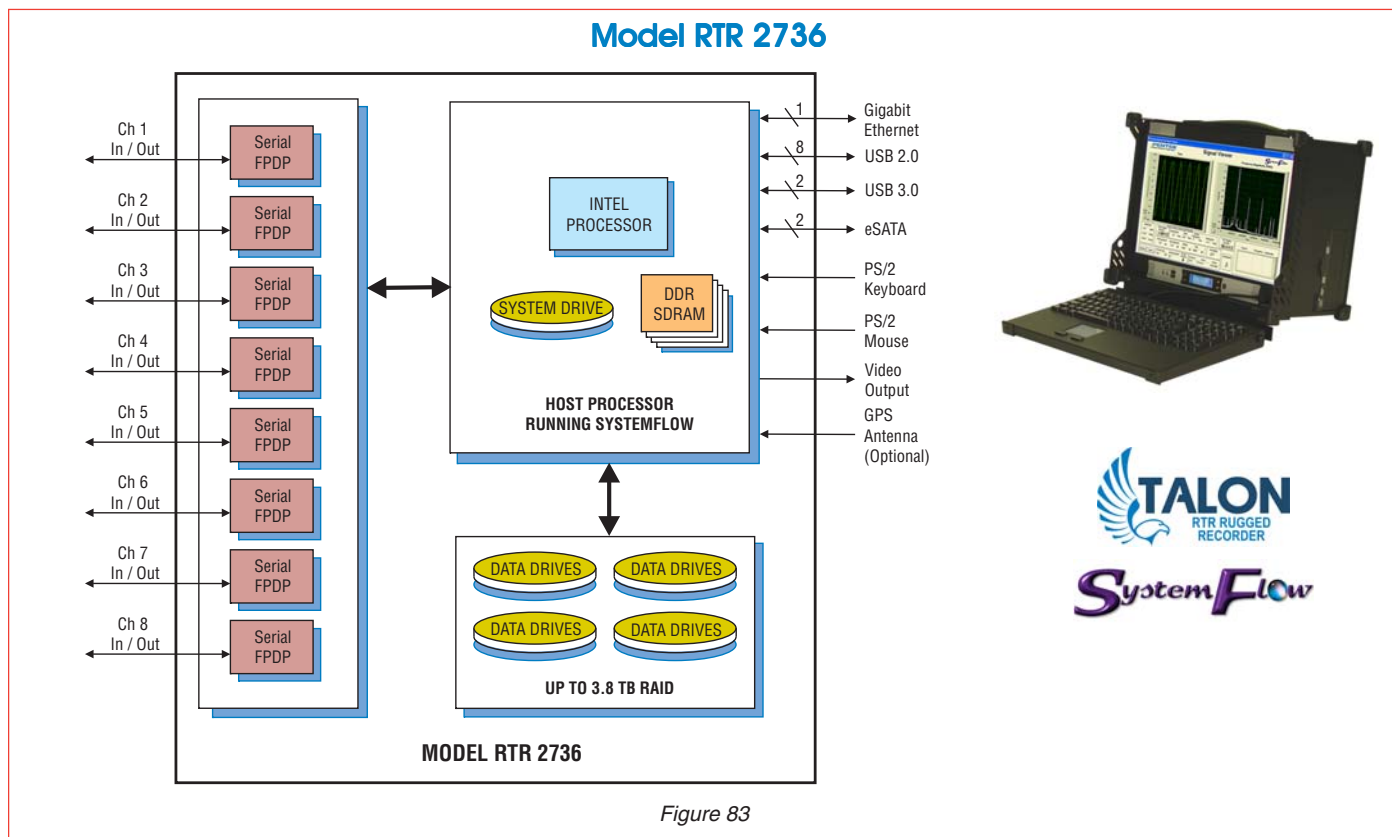
D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2727 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2727 performs well in ground, shipborne and airborne environments.

Products

Eight-Channel Serial FPDP Rugged Portable Recorder



The Talon RTR 2736 is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

The RTR 2736 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 200 MB/sec per serial FPDP link.

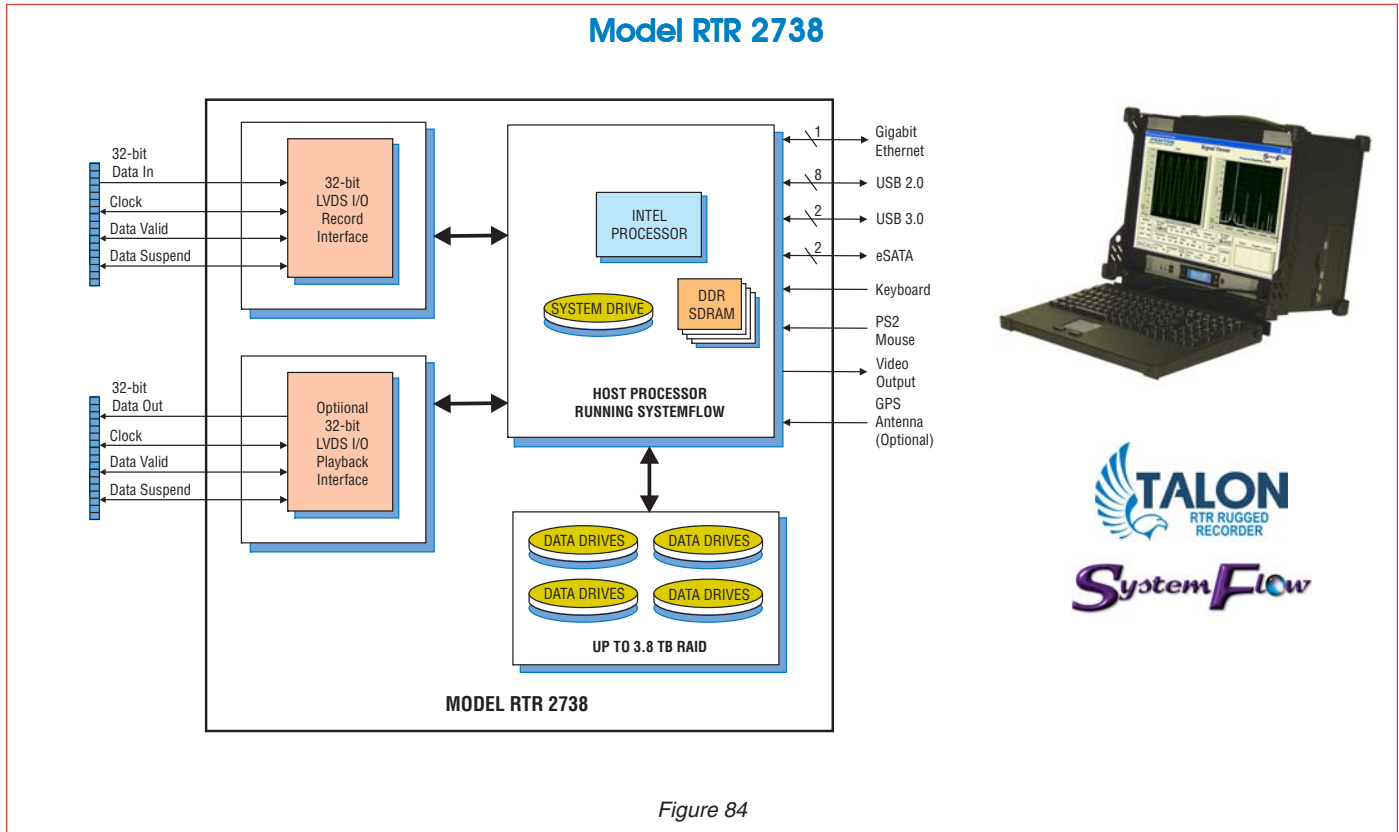
The RTR 2736 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2736 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide storage capacities of up to 3.8 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Products

LVDS Digital I/O Rugged Portable Recorder



The Talon RTR 2738 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the rugged, lightweight portable package achieves sustained recording rates of up to 1 GB/sec.

The RTR 2738 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2738 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

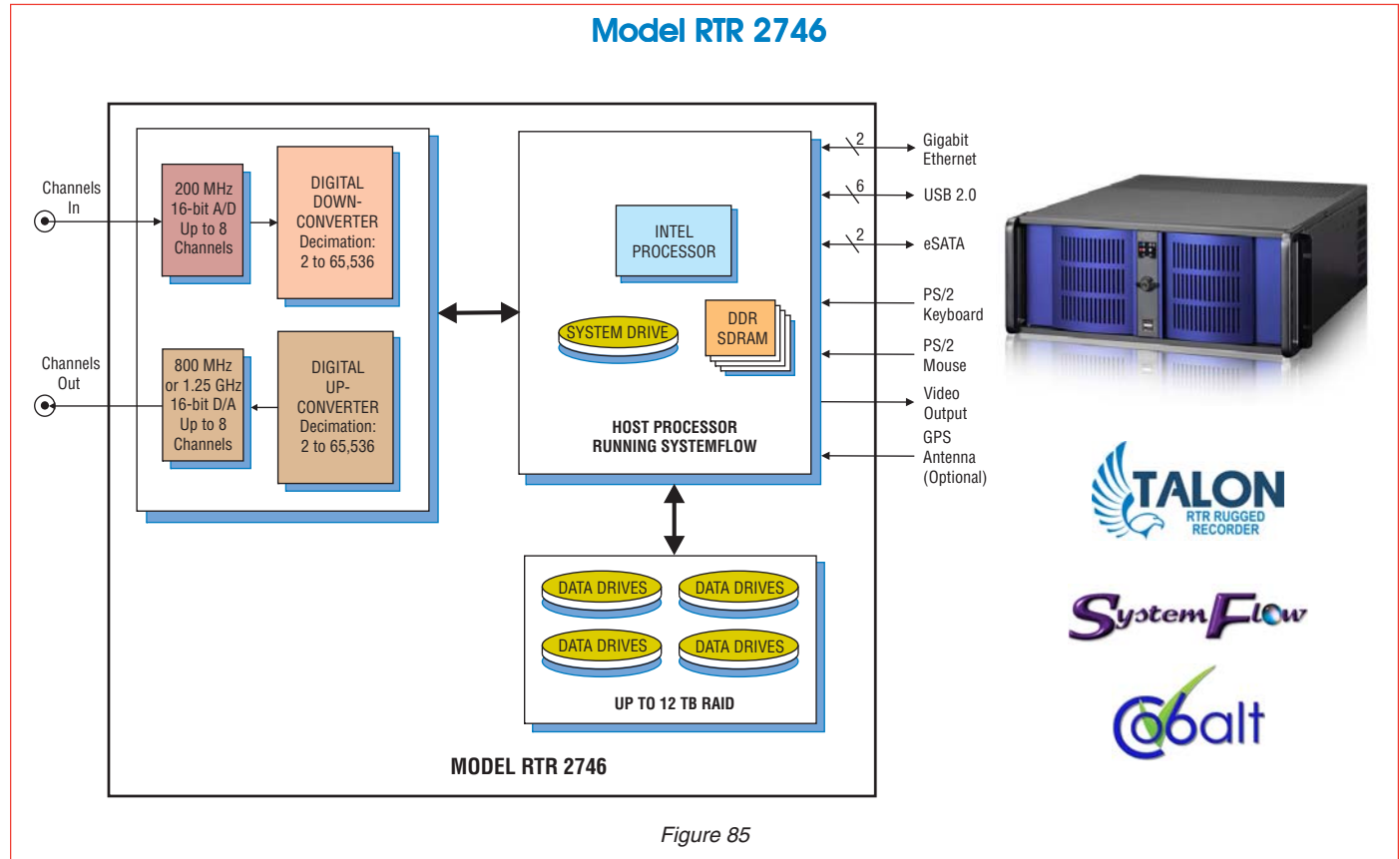
Built on a Windows 7 Professional workstation, the RTR 2738 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2738 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via a gigabit Ethernet port, eight USB 2.0 ports, two USB 3.0 ports or two eSATA 3 Ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD \pm R/RW drive.

The RTR 2738 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using shock- and vibration-resistant SSDs, the RTR 2738 is designed to reliably operate as a portable field instrument.

Products

Eight-Channel RF/IF 200 MS/Sec Rugged Rackmount Recorder



The Talon RTR 2746 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2746 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2746 can be configured to stream data to and from disk at rates as high as 2.0 GB/sec.

The RTR 2746 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz or 1.25 GHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system.

The 24 hot-swappable SSD's provide storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2746 performs well in ground, shipborne and airborne environments.

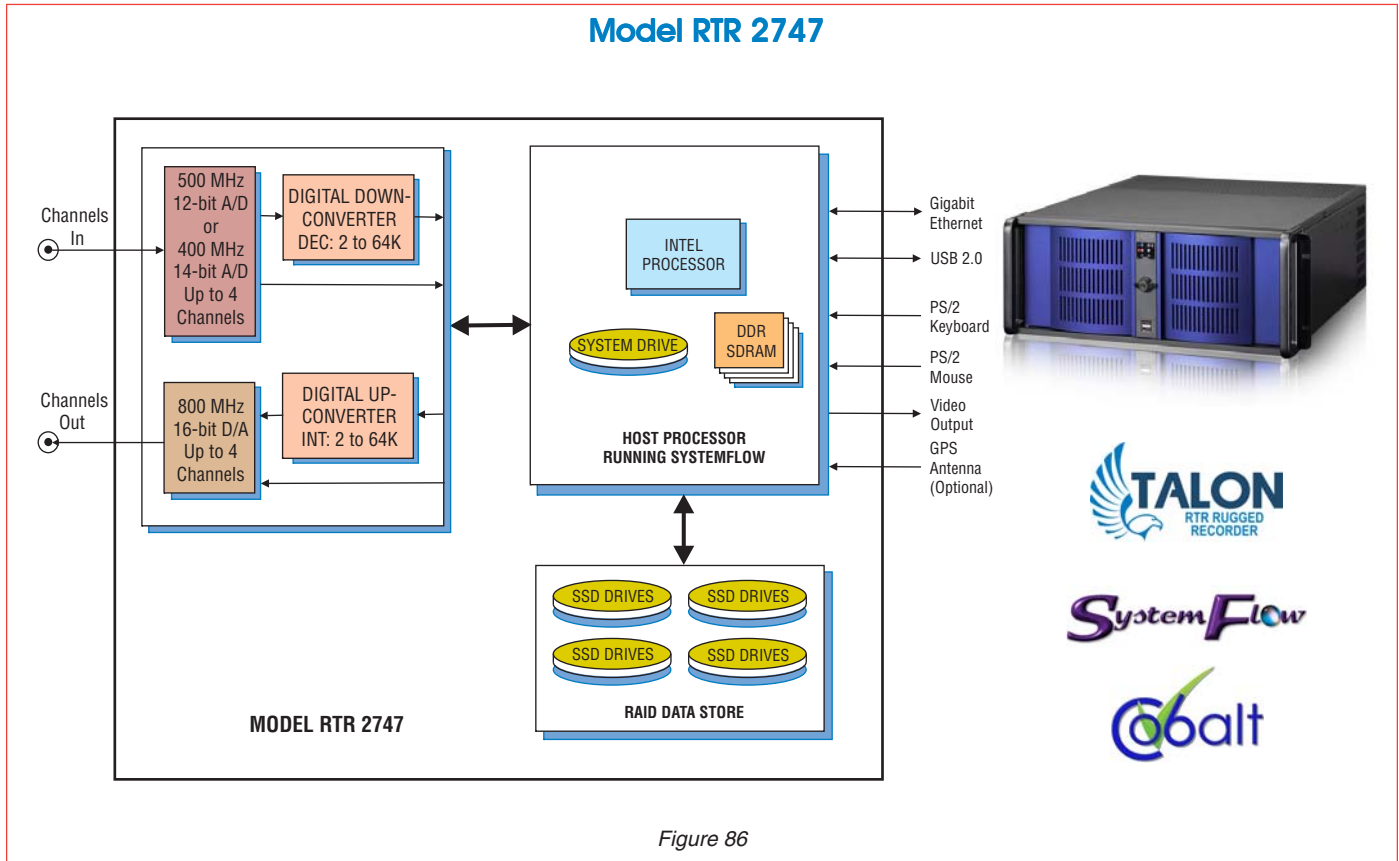
The RTR 2746 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Products

Four-Channel RF/IF 500 MS/Sec Rugged Rackmount Recorder



The Talon RTR 2747 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2747 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2747 can be configured to stream data to and from disk at rates as high as 4.0 GB/sec.

The RTR 2747 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system.

The hot-swappable SSD's provide storage capacity of up to 11.5 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2747 performs well in ground, shipborne and airborne environments.

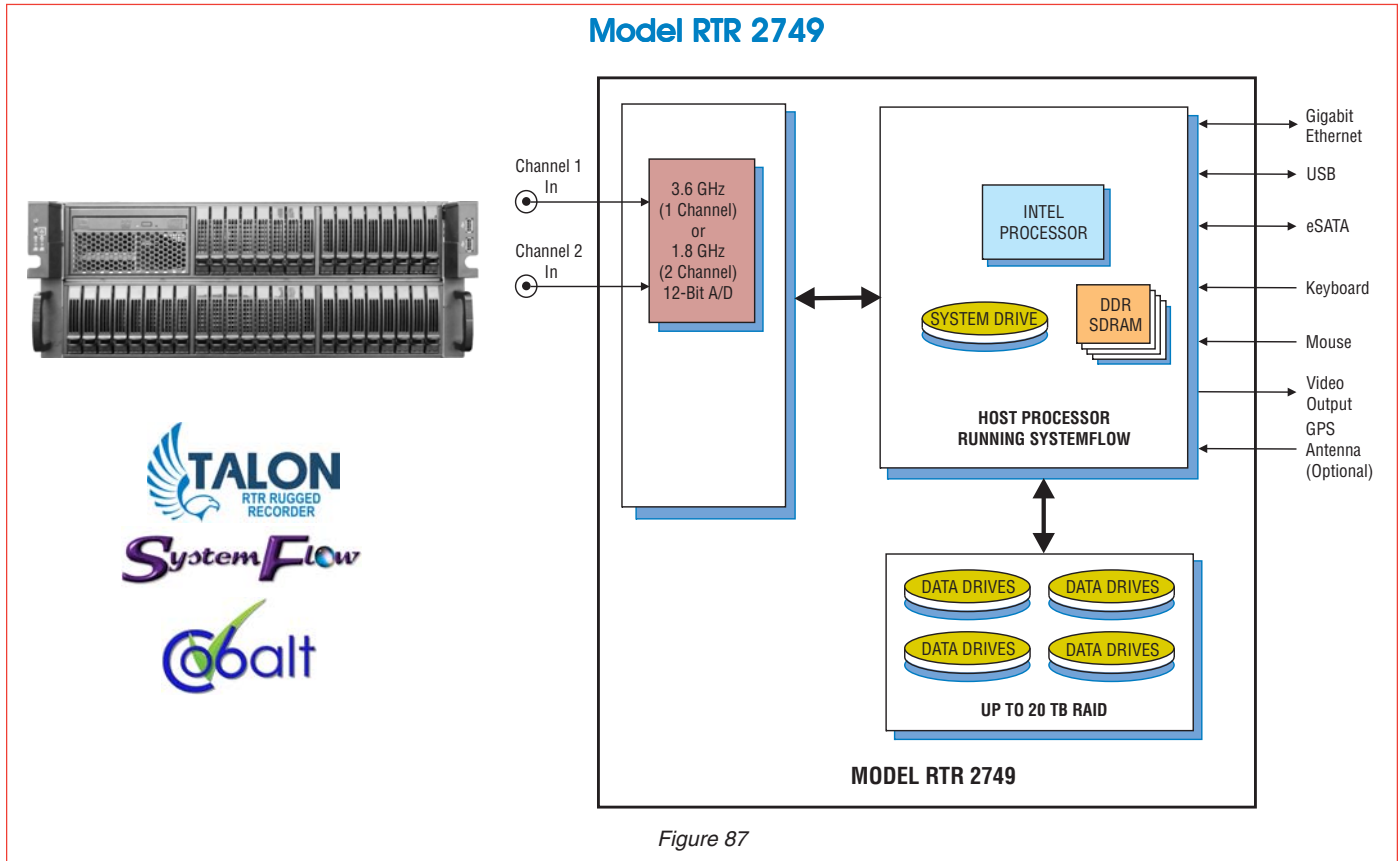
The RTR 2747 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Products

Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rugged Rackmount Recorder



Designed to operate under conditions of shock and vibration, the Talon RTS 2749 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2749 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3,200 MB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

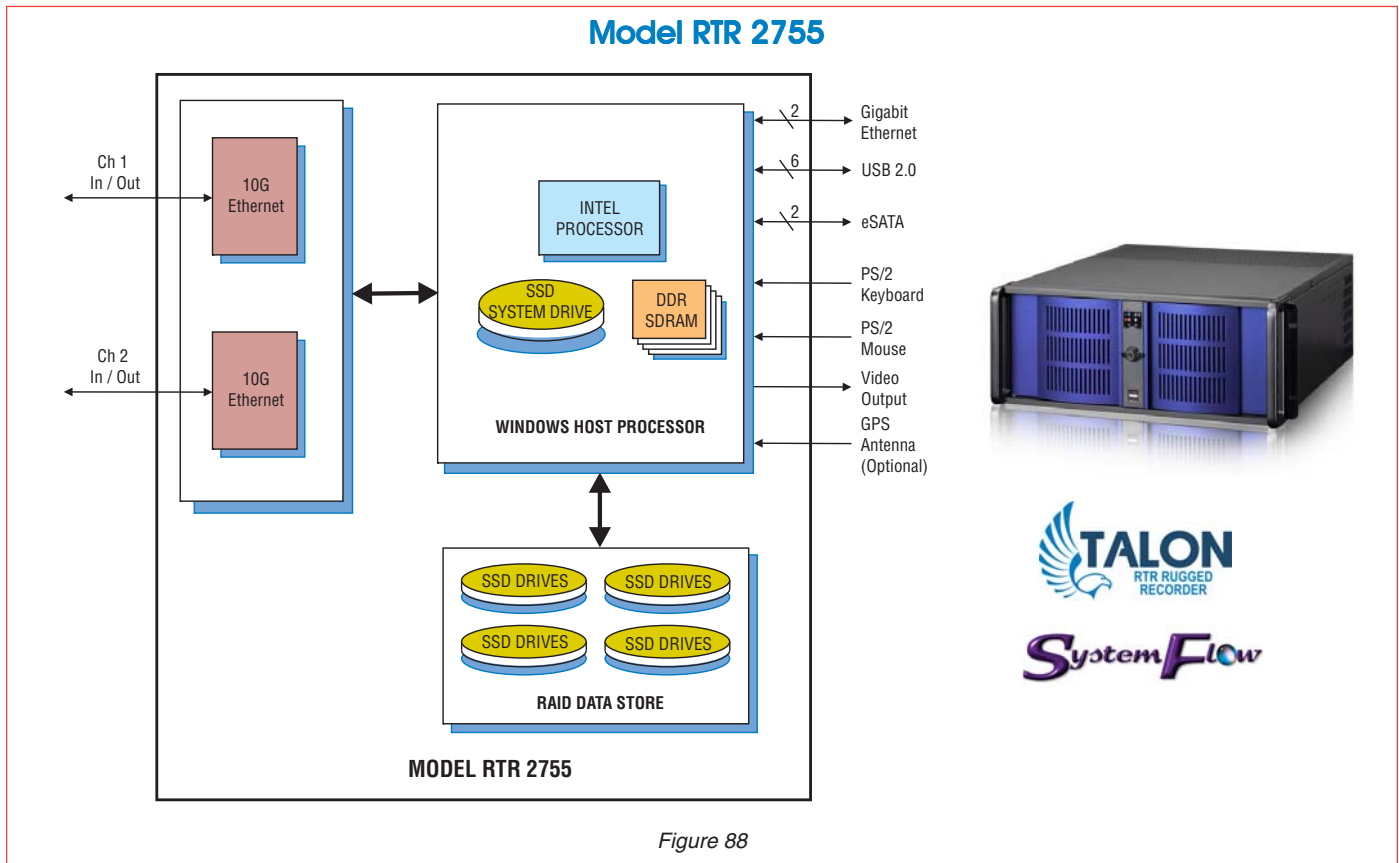
The RTS 2749 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system. Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2749 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2749 allows the user to install post processing and analysis tools to operate on the recorded data. The hot-swappable SSDs provide a storage capacity of up to 20 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2749 performs well in ground, shipborne and airborne environments.

Products

Two-Channel 10-Gigabit Ethernet Rugged Rackmount Recorder



Designed to operate under conditions of shock and vibration, the Talon RTR 2755 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized solid-state drive storage technology, the system guarantees loss-free performance at aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

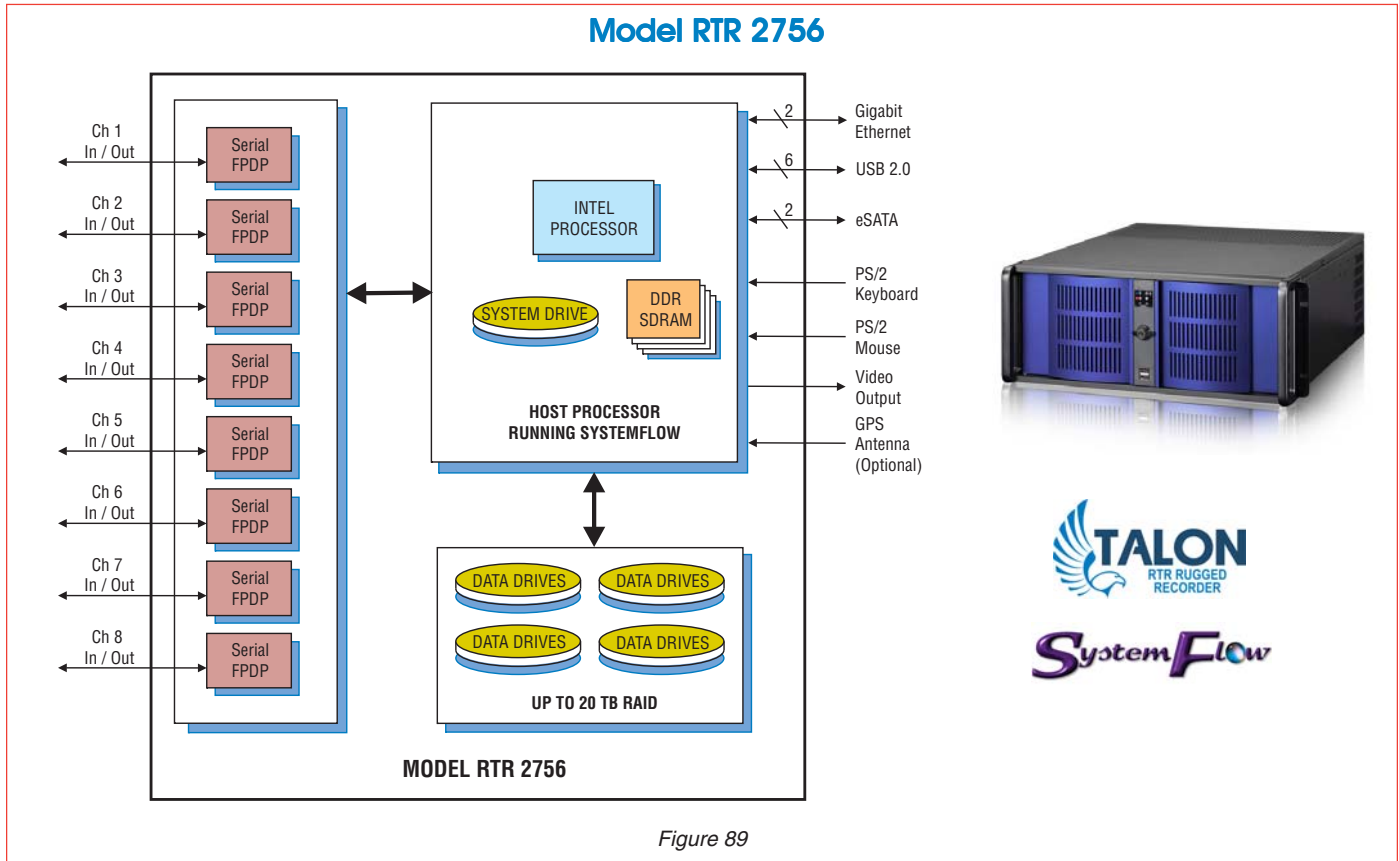
The RTR 2755 includes the SystemFlow Recording Software that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2755 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2755 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2755 performs well in ground, shipborne and airborne environments. The 24 hot-swappable SSD's provide a storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Products

Eight-Channel Serial FPDP Rugged Rackmount Recorder



Designed to operate under conditions of shock and vibration, the Talon RTR 2756 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2 GB/sec.

The RTR 2756 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

The RTR 2756 includes the SystemFlow Recording Software that provides an intuitive means to control the system.

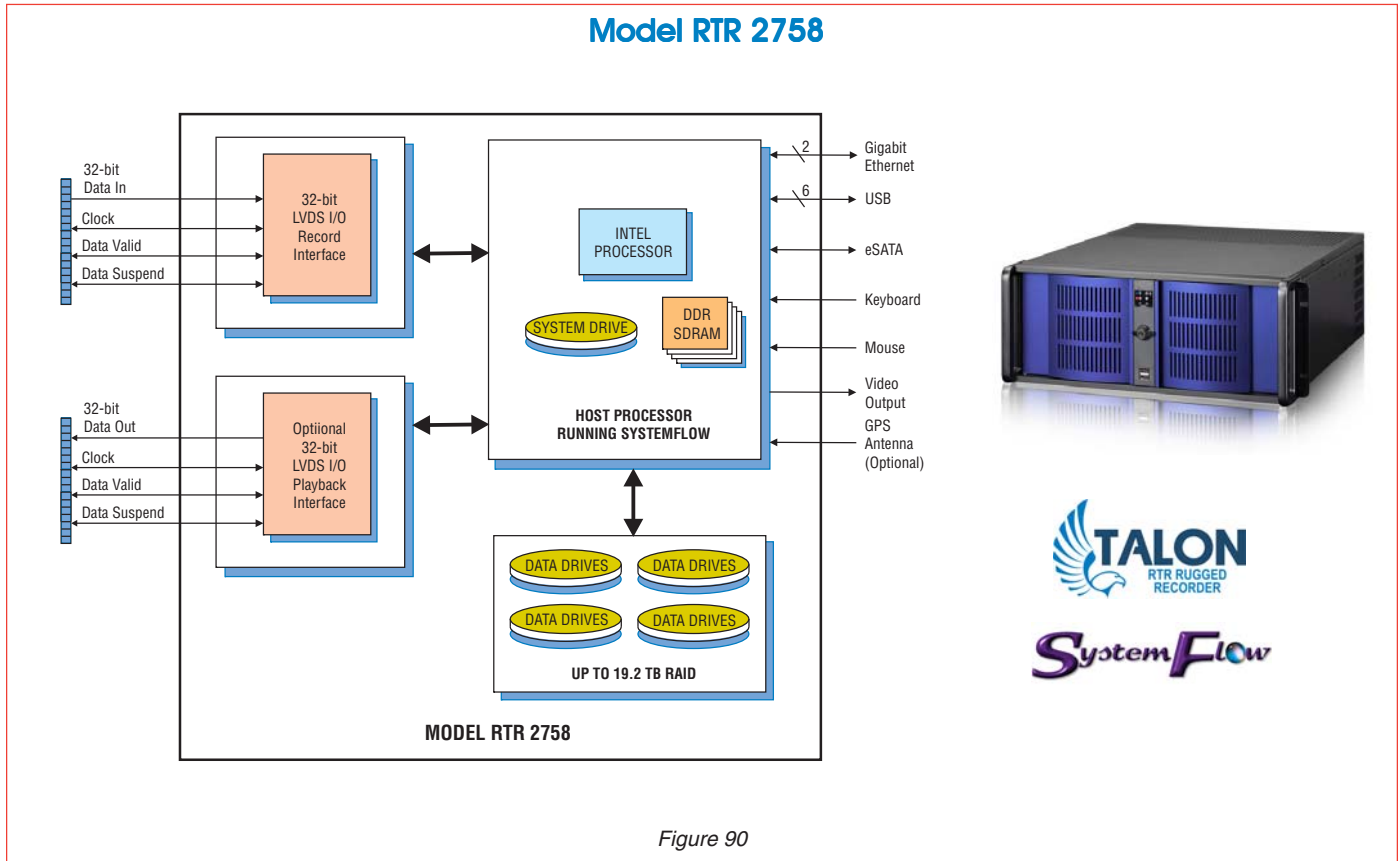
Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2756 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2756 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2756 performs well in ground, ship and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2756 can provide storage capacities of up to 19 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file's header.

Products

LVDS Digital I/O Rugged Rackmount Recorder



The Talon RTR 2758 is a complete turnkey system for recording and playing back digital data using a Pentek LVDS digital I/O board. Using highly optimized disk storage technology, the rugged rackmount system achieves sustained recording rates up to 1 GB/sec.

The RTR 2758 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2758 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

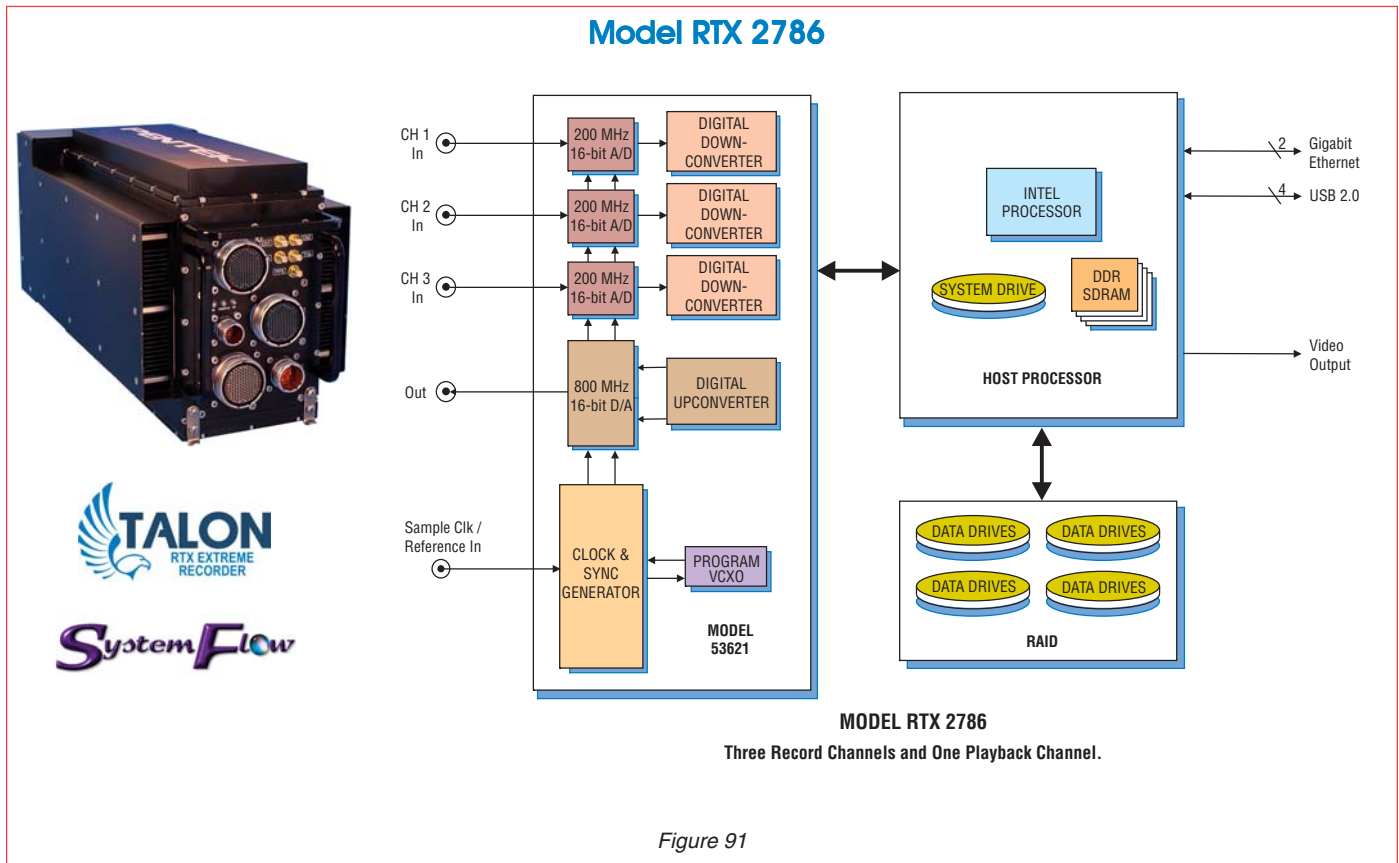
Built on a Windows 7 Professional workstation, the RTR 2758 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2758 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2758 performs well in ground, shipborne and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2758 can provide storage capacities of up to 19.2 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2758 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis that increase channel counts and aggregate data rates.

Products

Four-Channel RF/IF 200 MS/Sec Extreme 3U VPX Recorder



The Talon RTX 2786 is a turnkey, RF/IF signal recorder designed to operate under extreme environmental conditions. Housed in a ½ ATR chassis, the RTX 2786 leverages Pentek's 3U VPX SDR modules to provide a rugged recording system with up to four 16-bit, 200 MHz A/D converters with built-in digital downconversion capabilities. Optionally, the RTX 2786 provides one 800 MHz, 16-bit D/A converter with a digital upconverter for signal playback or waveform generation. As shown in the block diagram, the maximum number of record channels with this option is three.

The RTX 2786 uses conduction cooling to draw heat from the system components allowing it to operate in reduced air environments. It includes 1.92 TB of solid-state data storage, that allows it to operate with no degradation under conditions of extreme shock and vibration. The system is hermetically sealed and provides five D38999 connectors for power and I/O with four SMA connectors for analog I/O.

The RTX 2786 includes Pentek's SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

The user API allows users to integrate the recorder as a subsystem of a larger system. The API is provided as a C-callable library and allows for the recorder to be controlled over Ethernet, thus providing the ability to remotely control the recorder from a custom interface.

Four built-in solid-state drives provide reliable, high-speed storage with a total capacity of 1.92 TB.

Products

Pentek SystemFlow Recording Software for Analog Recorders

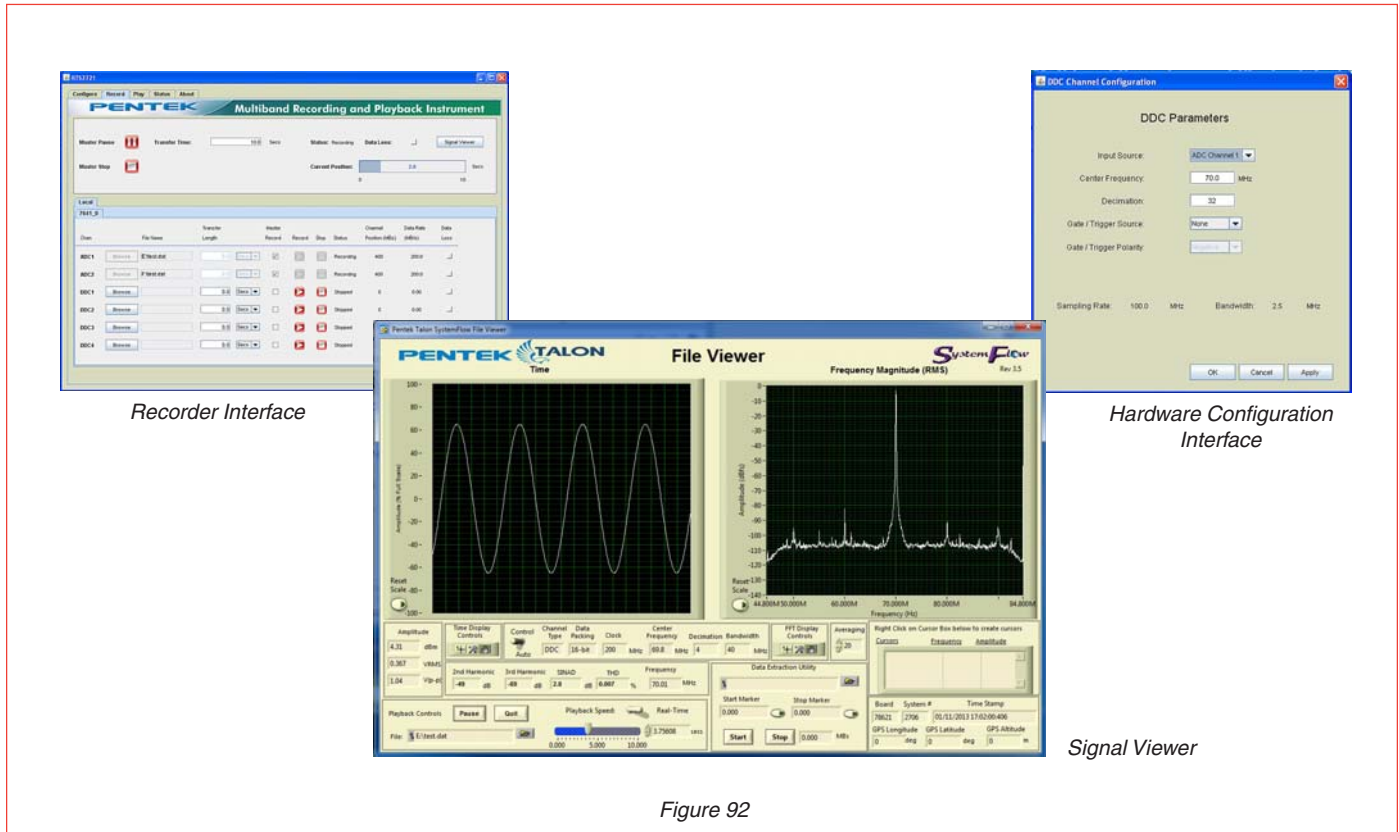


Figure 92

The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

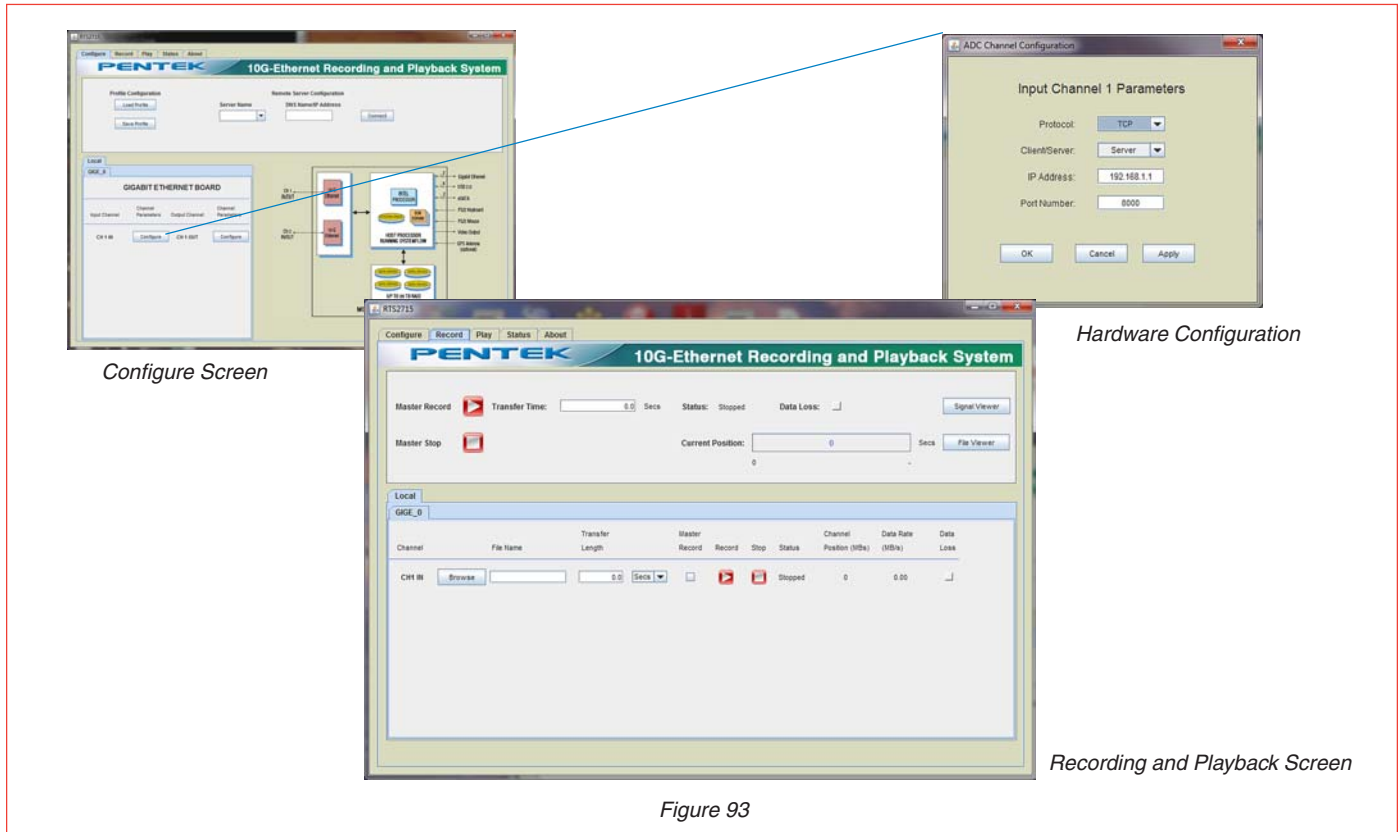
The **Hardware Configuration Interface** provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Products

Pentek SystemFlow Recording Software for Digital Recorders



The SystemFlow Software for Digital Recorders provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators.

The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The **Configure Screen** shows a block diagram of the system, and presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number.

The **Recording and Playback Screen** allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk-full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.

Applications

64-Channel Software Radio Recording System

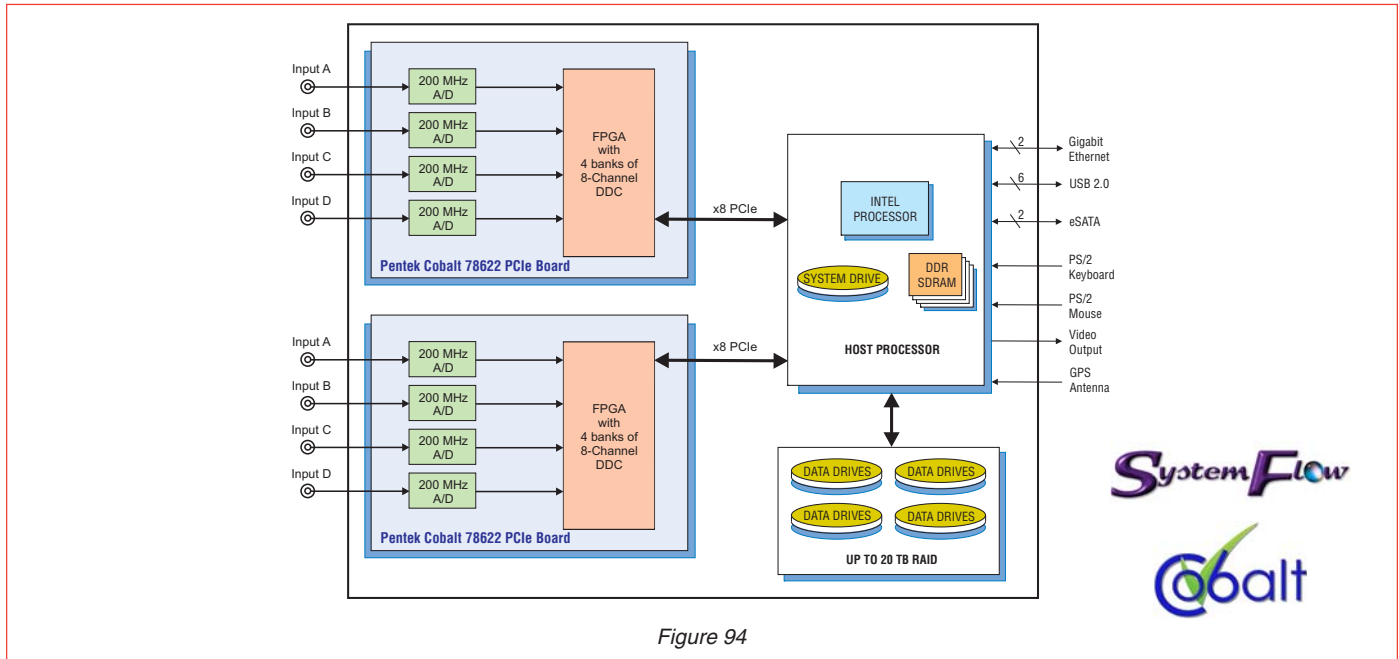


Figure 94

Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. All of the 8 channels within each bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel® Core™ i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Applications

L-Band Signal Processing System

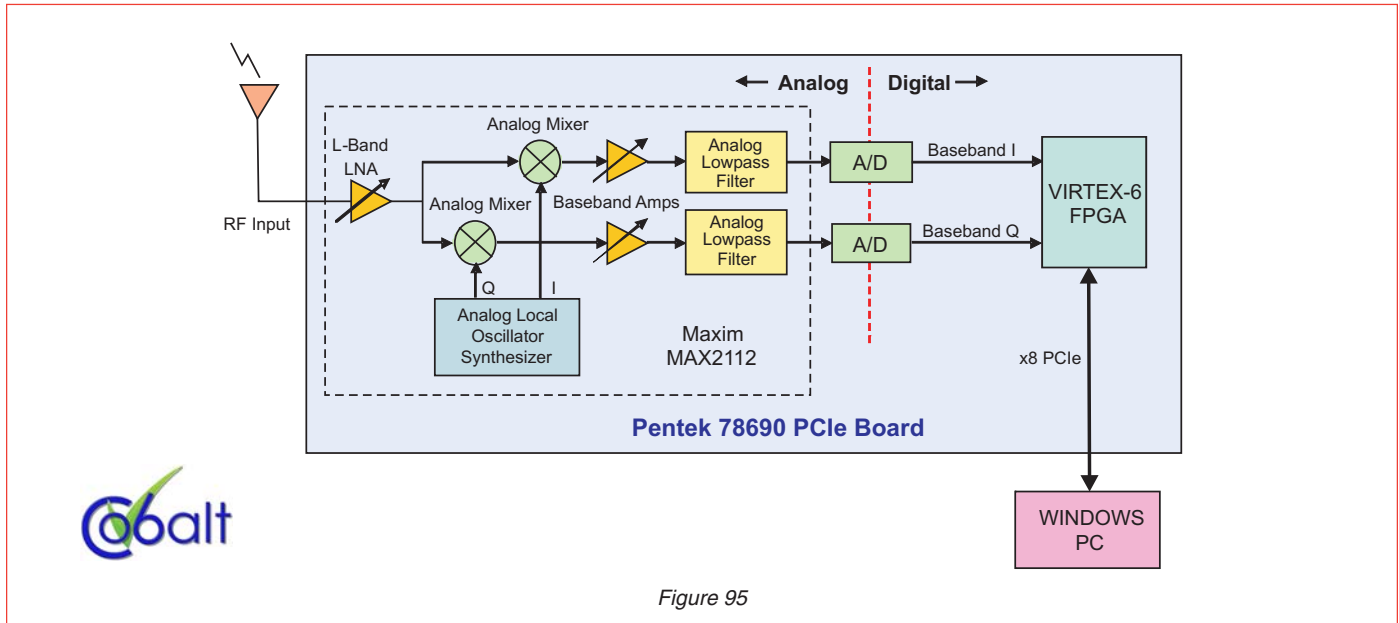


Figure 95

The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz. The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

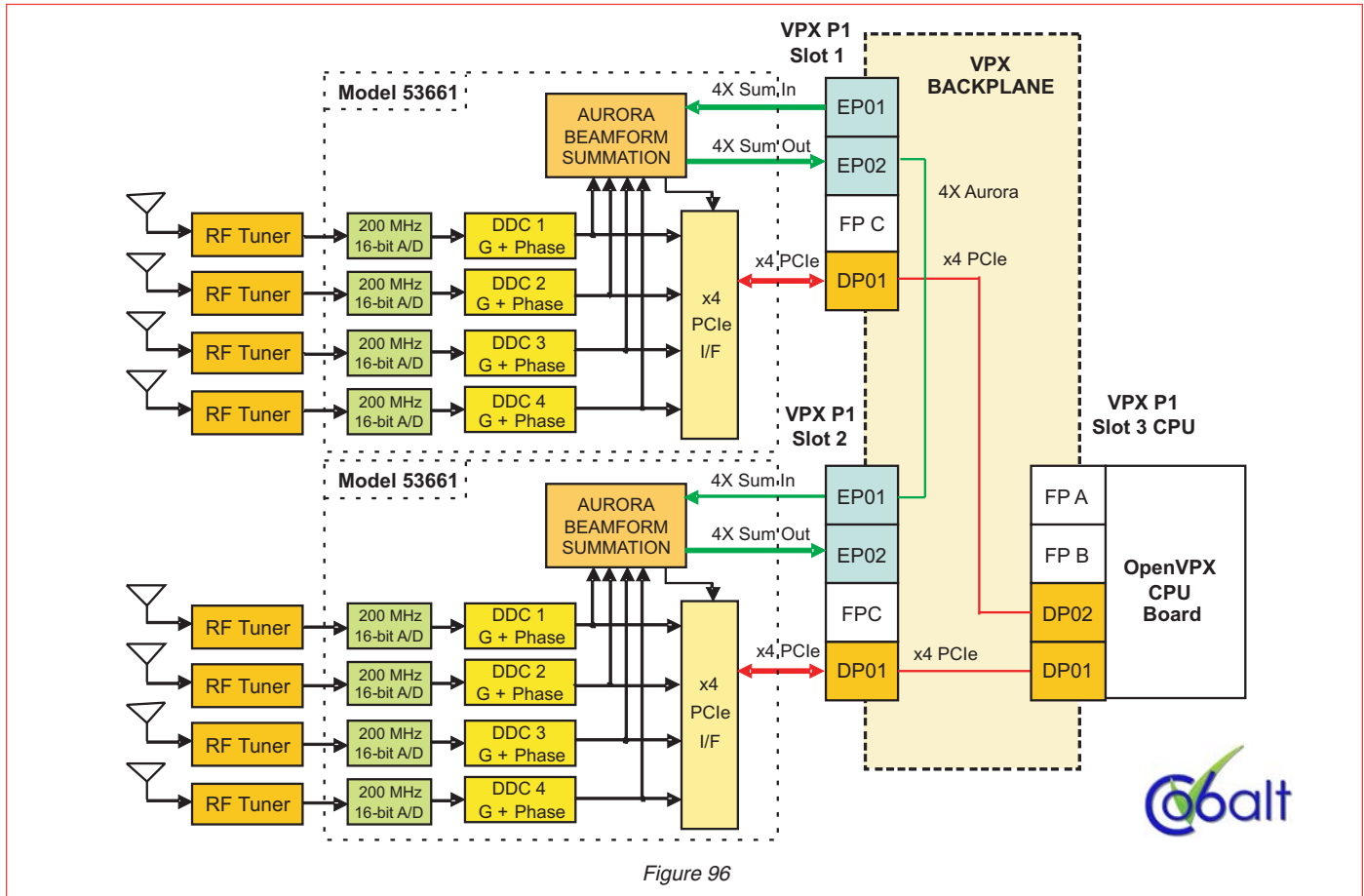
The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size addresses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.

Applications

8-Channel OpenVPX Beamforming System



Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX “fat pipes”.

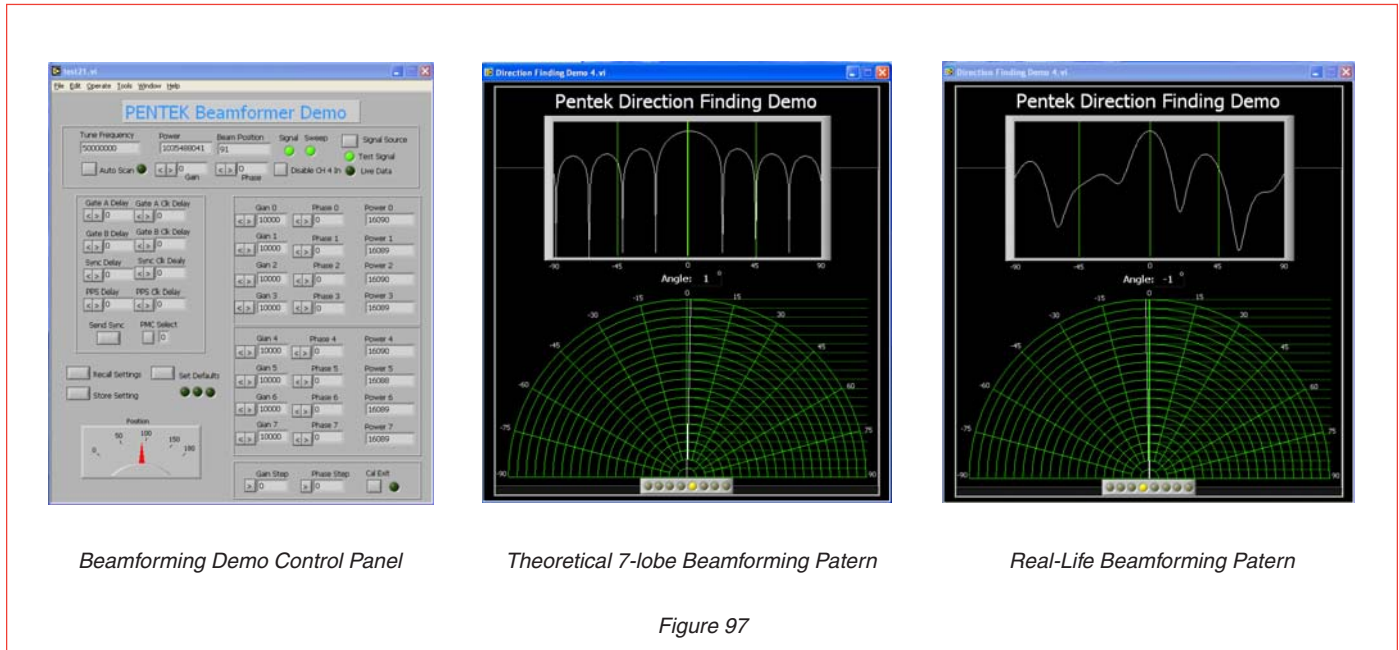
The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. ➤

Applications

8-Channel OpenVPX Beamforming Demo system



► Beamforming Demo System

The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum

sensitivity across arrival angles from -90° to $+90^{\circ}$ perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0° angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link:

[Beamforming Demo.](#)

Links



The following links provide you with additional information about the Pentek products presented in this handbook: just click on the model number. Links are also provided to other handbooks or catalogs that may be of interest to you in your development projects.

Model	Description	Page
4207	MPC8641 PowerPC Processor with Virtex-4 FPGA - VME/VXS	30
6822	Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS	31
6826	Dual 2 GHz, 10-bit A/D with Virtex-II Pro FPGAs - VME/VXS	32
7142	Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC	33
7242	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI	33
7342	Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI	33
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI	33
7742	Multichannel Transceiver with Virtex-4 FPGAs - Full-length PCIe	33
7842	Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe	33
5342	Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX	33
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC	34
7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 6U cPCI	34
7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U cPCI	34
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI	34
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length PCIe	34
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length PCIe	34
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX	34
7156	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC	35
7256	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI	35
7356	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI	35
7656	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI	35
7756	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe	35
7856	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe	35
5356	Dual 400 MHz 14-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX	35
7158	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC	36
7258	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI	36
7358	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI	36
7658	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI	36
7758	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe	36
7858	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe	36
5358	Dual 500 MHz 12-bit A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX	36
71620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC	37
78620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - PCIe	37
52620 & 53620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX	37
56620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC	37
72620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 6U cPCI	37
73620	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U cPCI	37
74620	6-Channel 200 MHz A/D, DUC, 4-Channel 800 MHz D/A, Two Virtex-6 FPGAs - 6U cPCI	37

More links on the next page ►

Links



Model	Description	Page
71720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - XMC	38
78720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - PCIe	38
52720 & 53720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX	38
56720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC	38
72720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 6U cPCI	38
73720	3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U cPCI	38
74720	6-Channel 200 MHz A/D, DUC, 4-Channel 800 MHz D/A, Two Virtex-7 FPGAs - 6U cPCI	38
—	GateXpress for FPGA-PCIe Configuration Management	39
78630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - PCIe	40
71630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - XMC	40
52630 & 53630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 3U VPX	40
56630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - AMC	40
72630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 6U cPCI	40
73630	1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 3U cPCI	40
74630	Two 1 GHz A/Ds, Two 1 GHz D/As, Two Virtex-6 FPGAs - 6U cPCI	40
72640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI	41
73640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U cPCI	41
74640	2-Channel 3.6 GHz and 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGAs - 6U cPCI	41
71640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC	41
78640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - PCIe	41
52640 & 53640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX	41
56640	1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC	41
52650 & 53650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX	42
71650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC	42
78650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - PCIe	42
56650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC	42
72650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 6U cPCI	42
73650	2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U cPCI	42
74650	4-Channel 500 MHz A/D, DUC, 4-Channel 800 MHz D/A, Two Virtex-6 FPGAs - 6U cPCI	42
71660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - XMC	43
78660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - PCIe	43
52660 & 53660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 3U VPX	43
56660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - AMC	43
72660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U cPCI	43
73660	4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGAs - 3U cPCI	43
74660	8-Channel 200 MHz 16-bit A/D with Two Virtex-6 FPGAs - 6U cPCI	43
71760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - XMC	44
78760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - PCIe	44
52760 & 53760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U VPX	44
56760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - AMC	44
72760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U cPCI	44
73760	4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U cPCI	44
74760	8-Channel 200 MHz 16-bit A/D with Two Virtex-7 FPGAs - 6U cPCI	44

More links on the next page ➤

Links



Model	Description	Page
71661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - XMC	45
78661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - PCIe	45
52661 & 53661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U VPX	45
56661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - AMC	45
72661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI	45
73661	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U cPCI	45
74661	8-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI	45
78662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - PCIe	46
71662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - XMC	46
52662 & 53662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U VPX	46
56662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - AMC	46
72662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI	46
73662	4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U cPCI	46
74662	8-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI	46
56670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC	47
71670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC	47
78670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - PCIe	47
52670 & 53670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX	47
72670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U cPCI	47
73670	4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U cPCI	47
74670	8-Channel 1.25 GHz D/A with DUCs, and Two Virtex-6 FPGAs - 6U cPCI	47
53690 & 52690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX	48
71690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC	48
78690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - PCIe	48
56690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - AMC	48
72690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U cPCI	48
73690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U cPCI	48
74690	Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and Two Virtex-6 FPGAs - 6U cPCI	48
71610	LVDS Digital I/O with Virtex-6 FPGA - XMC	49
78610	LVDS Digital I/O with Virtex-6 FPGA - PCIe	49
52610 & 53610	LVDS Digital I/O with Virtex-6 FPGA - 3U VPX	49
56610	LVDS Digital I/O with Virtex-6 FPGA - AMC	49
72610	LVDS Digital I/O with Virtex-6 FPGA - 6U cPCI	49
73610	LVDS Digital I/O with Virtex-6 FPGA - 3U cPCI	49
74610	LVDS Digital I/O with Virtex-6 FPGA - 6U cPCI	49
71611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - XMC	50
78611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe	50
52611 & 53611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX	50
56611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - AMC	50
72611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI	50
73611	Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA - 3U cPCI	50
74611	Digital I/O: Octal Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI	50

More links on the next page ➤

Links



Model	Description	Page
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME	51
6891	System Synchronizer and Distribution Board - VME	52
7190	Multifrequency Clock Synthesizer - PMC	53
7290	Multifrequency Clock Synthesizer - 6U cPCI	53
7390	Multifrequency Clock Synthesizer - 3U cPCI	53
7690	Multifrequency Clock Synthesizer - PCI	53
7790	Multifrequency Clock Synthesizer - Full-length PCIe	53
7890	Multifrequency Clock Synthesizer - Half-length PCIe	53
5390	Multifrequency Clock Synthesizer - 3U VPX	53
7191	Multifrequency Clock Synthesizer - PMC	54
7291	Programmable Multifrequency Clock Synthesizer - 6U cPCI	54
7391	Programmable Multifrequency Clock Synthesizer - 3U cPCI	54
7691	Programmable Multifrequency Clock Synthesizer - PCI	54
7791	Programmable Multifrequency Clock Synthesizer - Full-length PCIe	54
7891	Programmable Multifrequency Clock Synthesizer - Half-length PCIe	54
5391	Programmable Multifrequency Clock Synthesizer - 3U VPX	54
7192	High-Speed Synchronizer and Distribution Board - PMC/XMC	55
7892	High-Speed Synchronizer and Distribution Board - PCIe	55
5392	High-Speed Synchronizer and Distribution Board - 3U VPX	55
7292	High-Speed Synchronizer and Distribution Board - 6U cPCI	55
7392	High-Speed Synchronizer and Distribution Board - 3U cPCI	55
7492	High-Speed Synchronizer and Distribution Board - 6U cPCI	55
7893	System Synchronizer and Distribution Board - Half-length PCIe	56
7194	High-Speed Clock Generator - PMC/XMC	57
7894	High-Speed Clock Generator - PCIe	57
5294	High-Speed Clock Generator - 3U VPX	57
5694	High-Speed Clock Generator - AMC	57
7294	High-Speed Clock Generator - 6U cPCI	57
7394	High-Speed Clock Generator - 3U cPCI	57
7494	High-Speed Clock Generator - 6U cPCI	57
9190	Clock and Sync Generator for I/O Modules - Rackmount	58
9192	High-Speed System Synchronizer Unit - Rackmount	59
RTS 2706	Eight-Channel RF/IF 200 MS/sec Rackmount Recorder	60
RTS 2707	Four-Channel RF/IF 500 MS/sec Rackmount Recorder	61
RTS 2709	Ultra Wideband One- or Two-Channel RF/IF 3.2 GS/sec Rackmount Recorder	62
RTS 2715	Two-Channel 10 Gigabit Ethernet Rackmount Recorder	63
RTS 2716	Eight-Channel Serial FPDP Rackmount Recorder	64
RTS 2718	LVDS Digital I/O Rackmount Recorder	65

More links on the next page ►

Links



Model	Description	Page
RTR 2726	Four-Channel RF/IF 200 MS/sec Rugged Portable Recorder	66
RTR 2727	Two-Channel RF/IF 500 MS/sec Rugged Portable Recorder	67
RTR 2736	Eight-Channel Serial FPDP Rugged Portable Recorder	68
RTR 2738	LVDS Digital I/O Rugged Portable Recorder	69
RTR 2746	Eight-Channel RF/IF 200 MS/sec Rugged Rackmount Recorder	70
RTR 2747	Four-Channel RF/IF 500 MS/sec Rugged Rackmount Recorder	71
RTR 2749	Ultra Wideband One- or Two-Channel RF/IF 3.2 GS/sec Rugged Rackmount Recorder	72
RTR 2755	Two-Channel 10 Gigabit Ethernet Rugged Rackmount Recorder	73
RTR 2756	Eight-Channel Serial FPDP Rugged Rackmount Recorder	74
RTR 2758	LVDS Digital I/O Rugged Rackmount Recorder	75
RTX 2786	Four-Channel RF/IF 200 MS/sec Extreme 3U VPX Recorder	76
Handbooks, Catalogs and Brochures		
Click here	Software Defined Radio Handbook	
Click here	Putting FPGAs to Work in Software Radio Systems Handbook	
Click here	Critical Techniques for High-Speed A/Ds in Real-Time Systems Handbook	
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